

Fixturing

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Document Purpose: To provide the test engineer a guide in **Creating a Fixture Schematic** to be used on the RI 7100A tester.

Major Steps:

1. Generating a [DUT Functional Block Diagram](#).
2. Generating a [DIB Schematic Layout](#)
3. Generating a [Fixture Schematic](#)

Generating the DUT Functional Block Diagram:

To be effective in producing a working fixture the test engineer first needs to define the test needs of the **DUT**. A **Functional Block Diagram** for the purpose of assigning tester resources should then be the first step in the fixture generation process. A sample block diagram is shown below at [Figure 1](#). The diagram should reflect the bulleted items below and be agreed upon by the test engineer and the design engineer.

- DUT Pin outs
- Voltage, Current, State, or RF requirements for each DUT pin
- External circuitry requirements for each DUT pin.
- Resource types and levels required for each pin (ie. RF, Static Digital, Digital Programming, DC voltages, etc...)

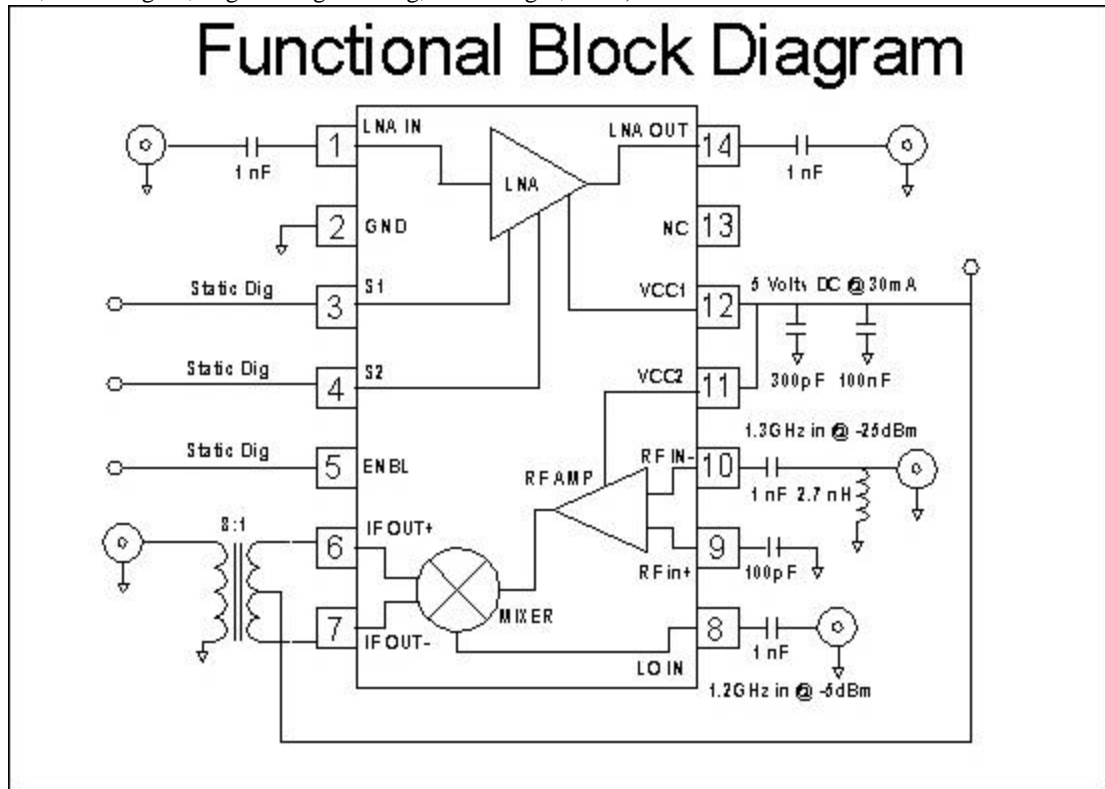


Figure 1
Functional Block Diagram

Generating the DIB Schematic Layout:

Once the part requirements are understood then the test engineer can begin to define the **Device Interface Board (DIB)** using these requirements. This process helps to do the following things:

- Define the **Fixture Top Assembly** required.
- Define the **Device Interface Board I/Os**.
- Define the **Fixture Carrier Board** and its type (**Active** vs **Passive**).
- It should also help to define the **Socket Type** required for the DUT.
- Define the routing of resource lines to the DUT from the edge of the **DIB**.

An example of a completed **DIB Schematic** is shown below in [Figure 2](#).

Steps :

1. Procure a copy of the standard **DIB Board Template** to see the actual pogo pin and RF launch positions.
2. Superimpose a DUT outline drawing onto it to see how the DUT pin outs relate to these positions.
3. Begin connecting with a pencil the DUT pins and the specific pogo pin and RF launch positions desired.
4. Keep in mind that specific tester resources do not need to be identified at this time. Also at this time it would be advisable to begin thinking of component placement as well.
5. Record the DUT pin numbers, function, and launch designation using a spread sheet program.
6. The **DUT Interface Board** can potentially be started at this time since the pogo pin locations and the RF launch positions are still independent of tester resources.

DIB Schematic

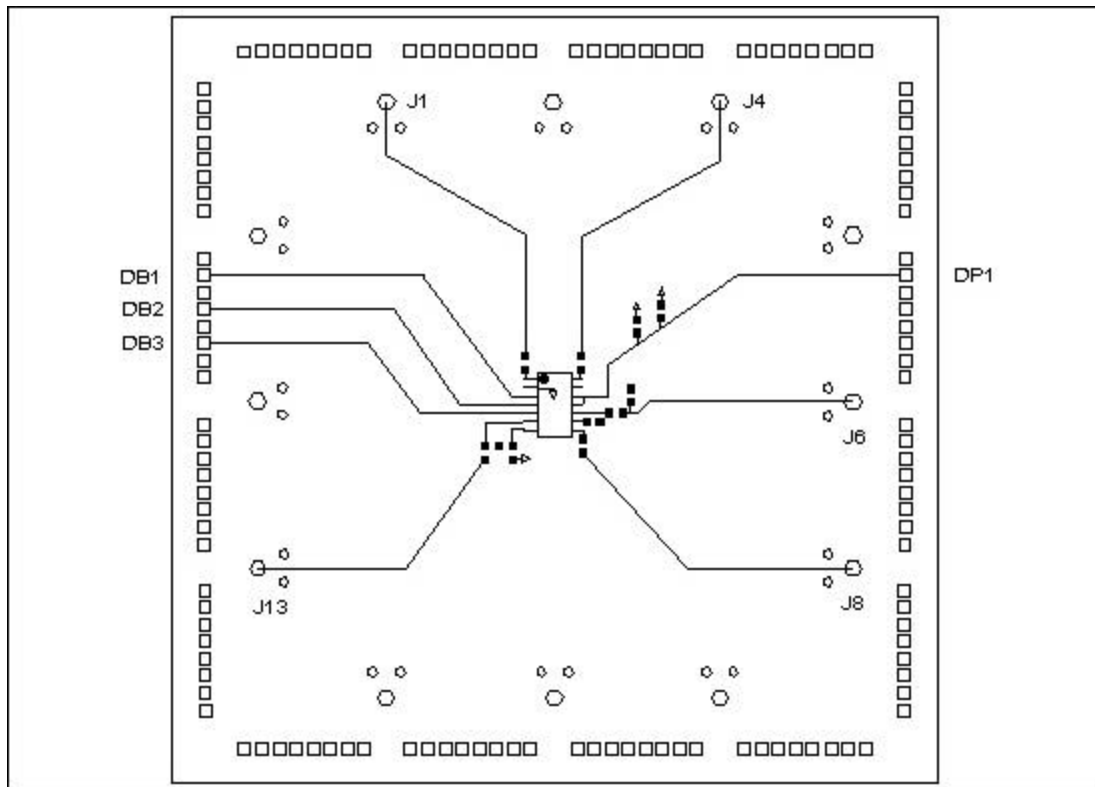


Figure 2
DIB Schematic

Generating the Fixture Schematic(Using the Fixture Carrier Board)

After determining the DIB I/Os then the test engineer can define the **Fixture Carrier Board**. This step should help the engineer to make the required connections between the DIB and the Fixture Carrier Board. It should also finish with the RF connections of the **Fixture Top Assembly** to the **Fixture Bottom Assembly**. This procedure will help the engineer to:

- Define potential **Fixture Modules** needed to test the part.
- Provide an understanding as to what **RF switching** may be needed.

Steps :

1. Obtain a copy of the **Fixture Carrier Board Template**.
2. Associate with each pogo pin position on the DIB Schematic a specific test head resource as found on the **Fixture Carrier Board Template**. As this is done, write them down on the DIB Schematic as shown in **Figure 2**.
3. Associate with each RF connection a position on the **Fixture Top Plate**. These can be found by referring to the **J1-J16** numbers around the periphery of the inside cut out of the board. When doing this make sure to remember that your **DIB Schematic** is upside down in relation to the printed side of the Fixture Carrier Board. Also remember that the **Fixture Carrier Board** can only be oriented correctly in one direction to the **Fixture Top Plate**.
4. The **J** numbers are associated with an **RF** interface at the top of the fixture. These numbers need to be associated with specific RF ports found on the **Test Head** itself. An RF switch needs to be added to the fixture any time a specific **Test Head RF Port** shows up more than once on the diagram. In the example in **Figure 2**, **RF Test Head Port 3** shows up twice requiring a **RF switch** between these two points and the test head. **Figure 3** represents the finished **Fixture Schematic**.

Fixture Schematic

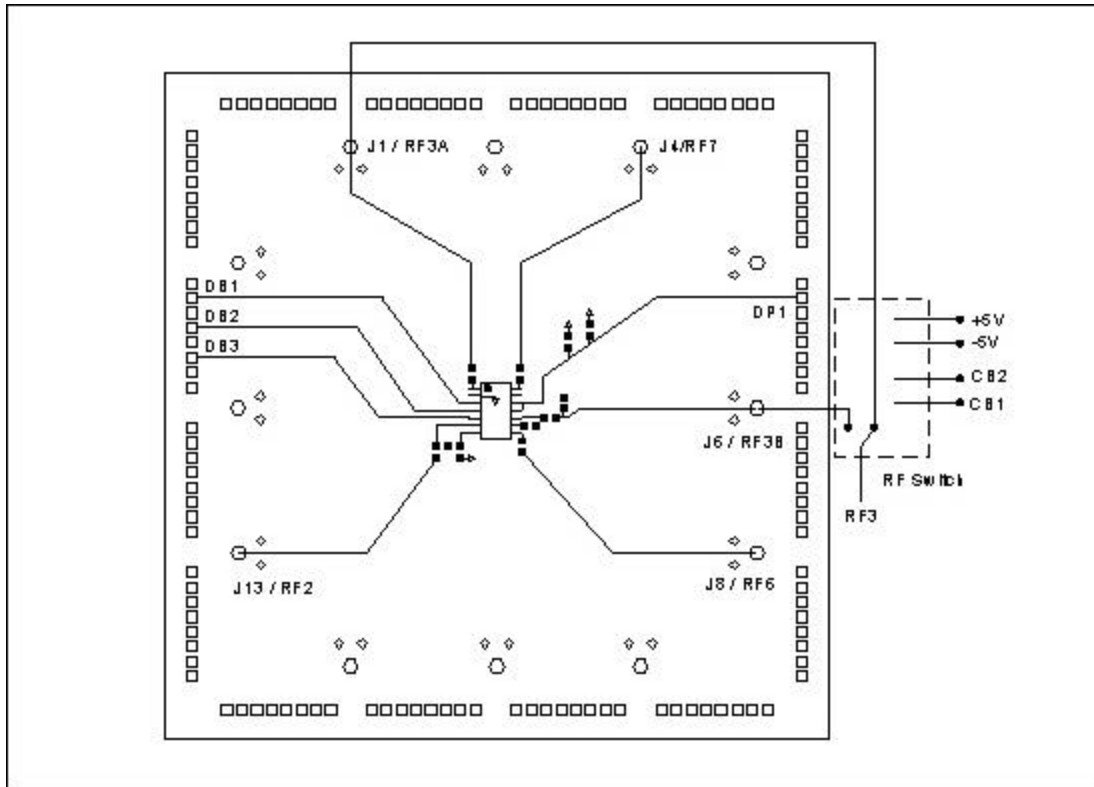


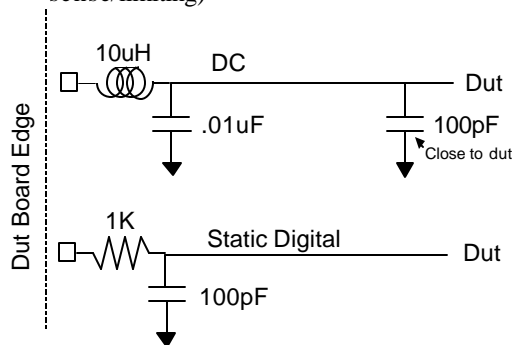
Figure 3
Fixture Schematic



Purpose:

The purpose of this document is to provide the test engineer with guide lines for DIB layout and design. These guidelines are intended to be used with boards to be used with the ROOS standard format test fixture interface.

- 1.) Use 0402s under the part, for close decoupling.
- 2.) End all DC traces in a 10uH inductor (noise suppression) and 0.01uF plus optional 100pF (close to dut), caps (shunt). Do not use caps larger than .1uF. Power VI cannot use inductor input (due to sense/limiting)



- 3.) Static digital use 1K Ohm series, 100pF shunt.
- 4.) Don't forget to hook up the ground return.
- 5.) Put in the serial number chip (and power for it).
- 6.) DC trace 8 mil minimum
- 7.) DC space 6 mil minimum
- 8.) Vias are to be 10mil minimum
- 9.) Pads are to be 26mil minimum
- 10.) RF trace 15 mil (50 ohm, on 8 mil Duroid). Do not break the ground plane under or over any RF trace.
- 11.) For precise RF use Rogers 8 mil Duroid 4003. FR4 is fine otherwise to 2.5GHz
- 12.) Use our "recipe" at Brothers Union International 408 749 8811 hard gold etc... Be very careful on the plating spec.
- 13.) The calibration board to be the same layout without matching components.
- 14.) Carefully locate Pin 1. See document [Fixture Carrier board Alignment/Orientation](#)
- 15.) Use layout nomenclature to match the fixture system for easy debug. See document [DIB Board Template](#)
- 16.) If using on-dutboard signal conditioning (i.e., Video/Differential Buffer) consider routing intermediate signals for calibration purposes
- 17.) Document the fixture and dutboard with a [Fixture Net List](#)



The RIK0006B Kit consists of two, dual SPDT RF switch modules, for a total of four SPDT switches. The switches are attached in the test fixture by standard 3M double sided adhesive tape. The unused port retrun loss is reflective in nature.

Figures / Tables:

- [Figure 1](#) : Physical representation of the Switch Top Side view.
- [Table 1](#) : Pin Out
- [Table 2](#) : Typical Performance
- [Figure 2](#) : RF Default Conditions
- [Figure 3](#) : Insertion Loss Measurement.
- [Figure 4](#) : Isolation Measurement / Common to Inactive Port.
- [Figure 5](#) : Isolation Measurement / Active to Inactive Port.
- [Figure 6](#) : Return Loss Common Port
- [Figure 7](#) : Return Loss Active Port
- [Figure 8](#) : Picture

Figure 1
Top Side View

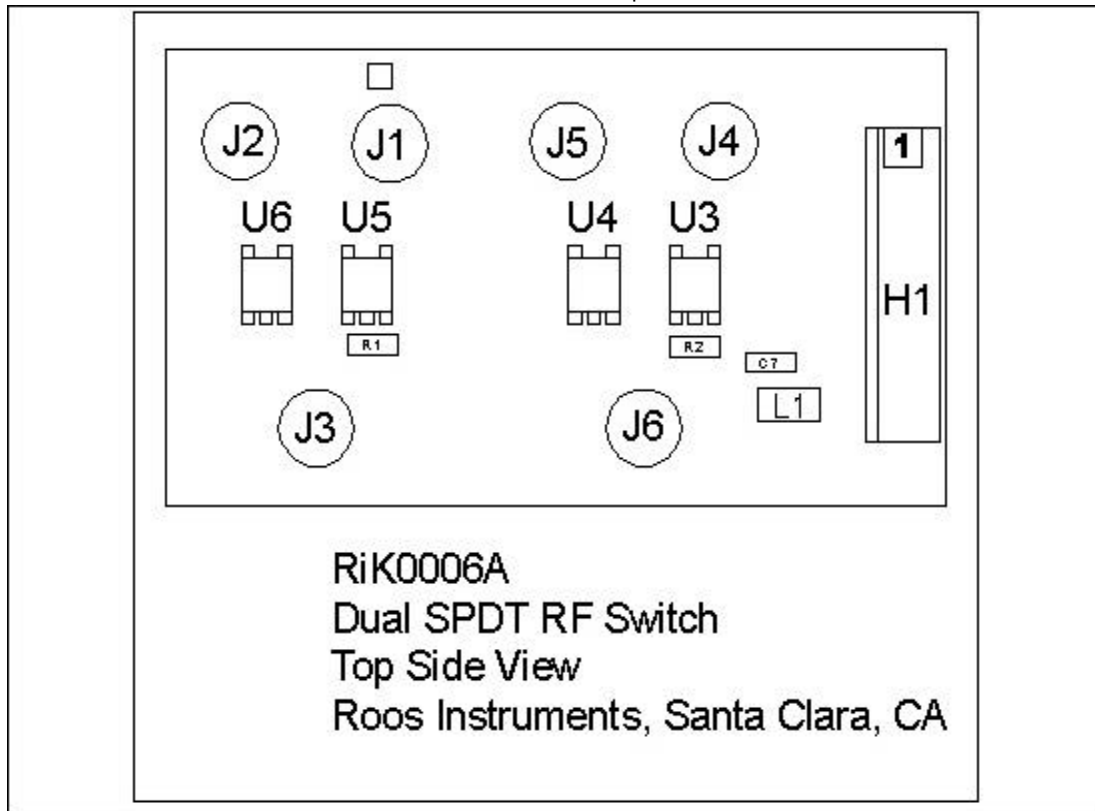


Figure 1
Top Side View

RiK0006A SPDT Switch Pin Out

Description	Connection	Type	Notes
+5V Supply	H1-7 & 8	Header Pin	
Switch 1 Control	H1-3	Header Pin	
Switch 2 Control	H1-6	Header Pin	
Ground	H1-4/5		
Switch 1, Pole	J3	MCX Female	DC Blocked
Switch 1, NC	J1	MCX Female	DC Blocked
Switch 1, NO	J2	MCX Female	DC Blocked
Switch 2, Pole	J6	MCX Female	DC Blocked
Switch 2, NC	J4	MCX Female	DC Blocked
Switch 2, NO	J5	MCX Female	DC Blocked

Table 1
Pin Out

Switch 1 & 2 Typical Performance

Current Draw +/-5V All CBITs High	100uA typical
Current Draw +/-5V One CBIT Low	1.5mA typical
Current Draw +/-5V Two CBITs Low	3mA typical
Insertion Loss (Activated)	Fig. 3
0.5dB Point (low end)	1Kz typical
3.0dB Point (low end)	400Hz typical
Max Frequency	2.5GHz
Isolation / Pole to Inactive	Fig. 4
Isolation NC to NO	Fig. 5
Common Port Return Loss	Fig. 6
Active Port Return Loss	Fig. 7

Table 2
Typical Performance

S21 FORWARD TRANSMISSION

LOG MAGNITUDE

REF=0.000 dB

2.000 dB/DIV

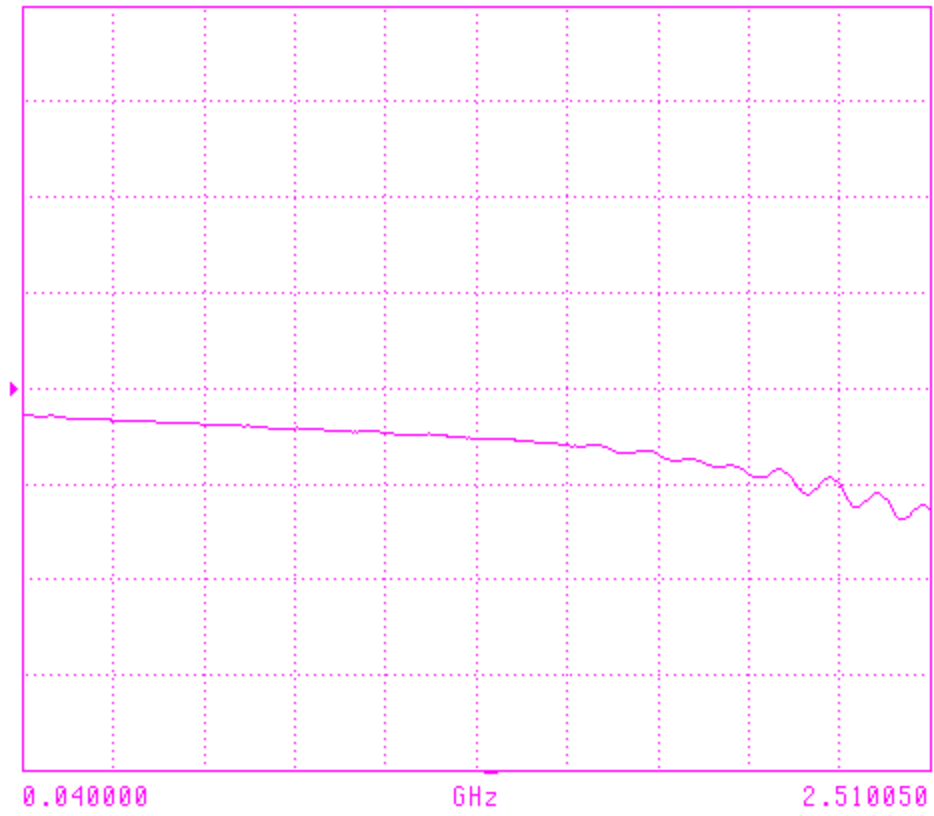


Figure 3
Insertion Loss

Isolation Common to Unused Port

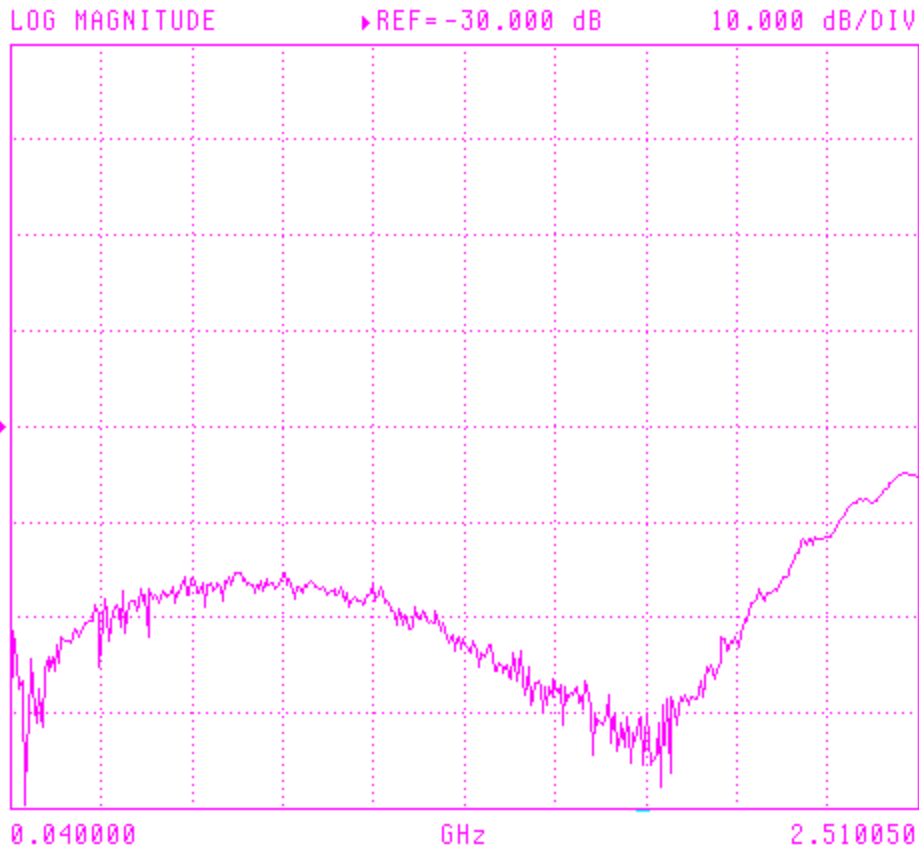


Figure 4
Isolation Common to Inactive Port

Isolation NC to NO Port

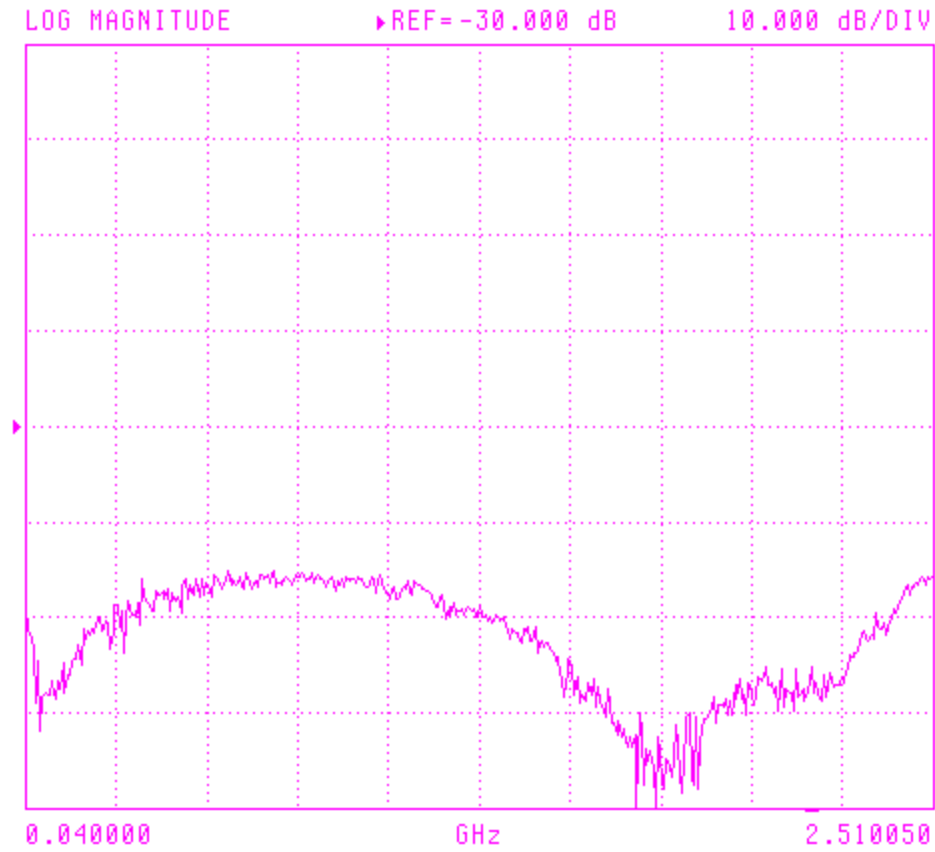


Figure 5
Isolation Active to Inactive Port

S11 FORWARD REFLECTION

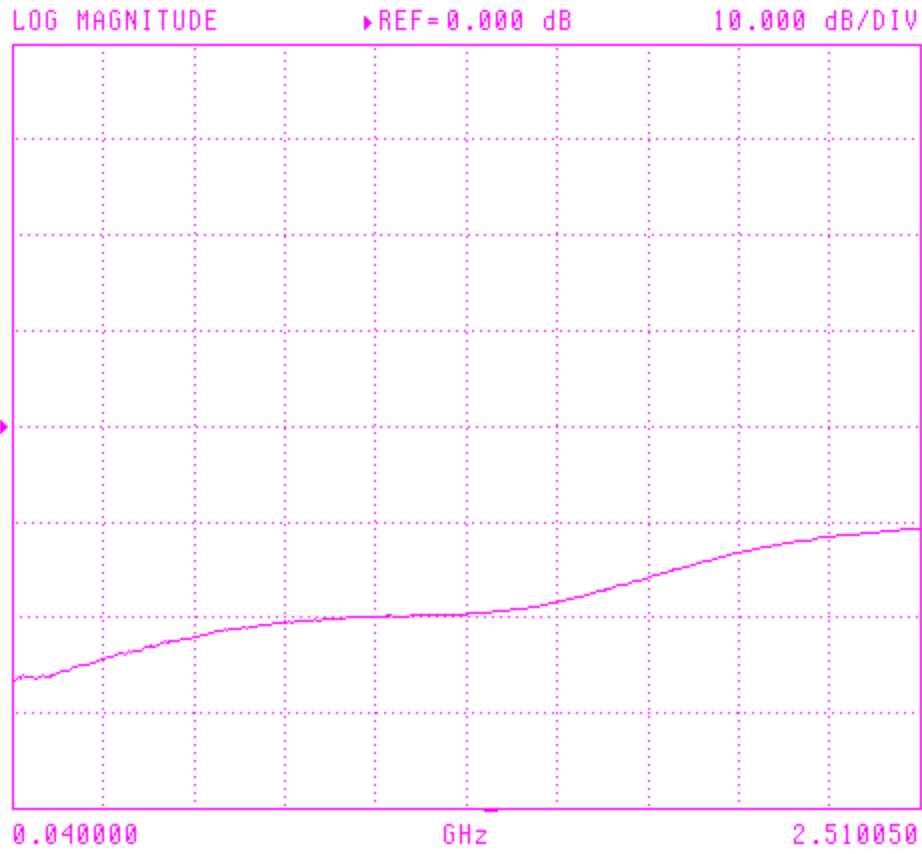


Figure 6
Common Port Return Loss

S22 REVERSE REFLECTION

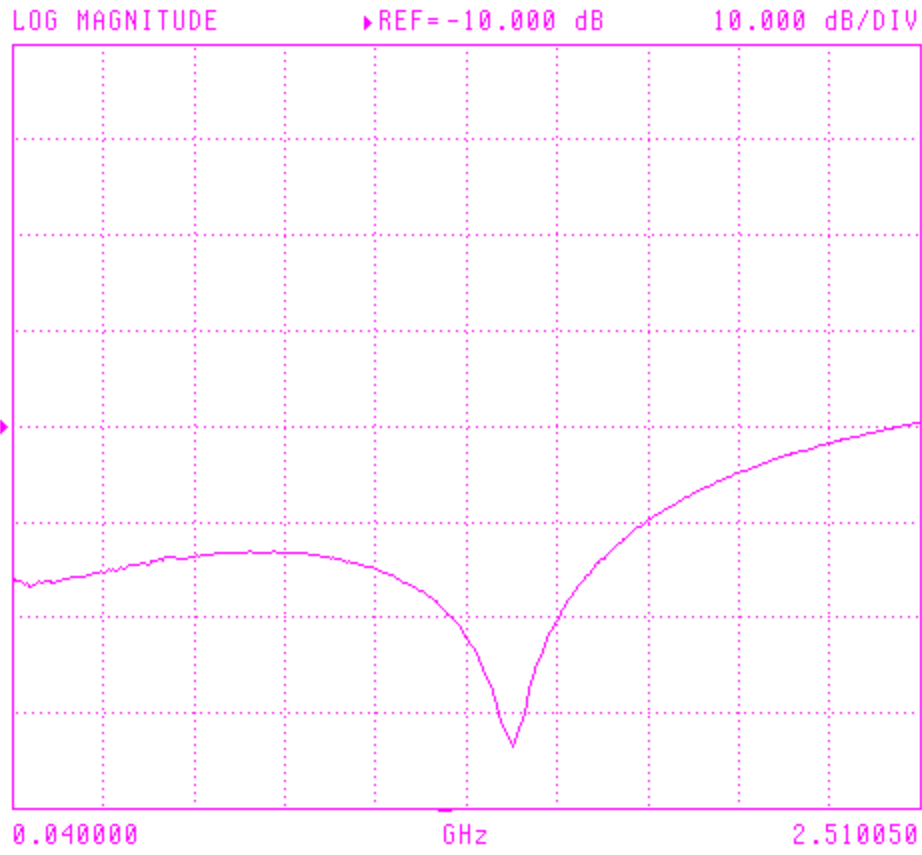


Figure 7
Active Port Return Loss

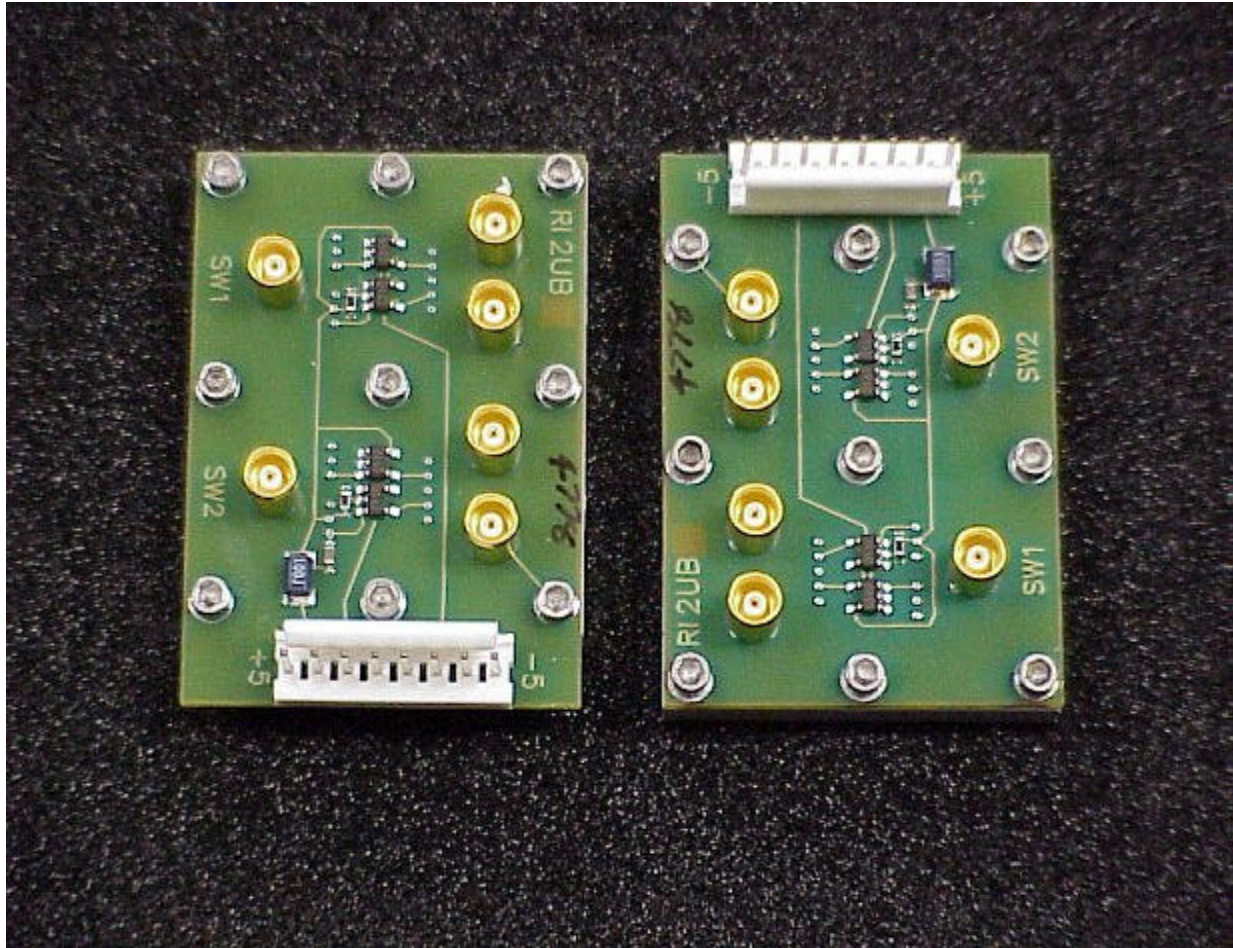
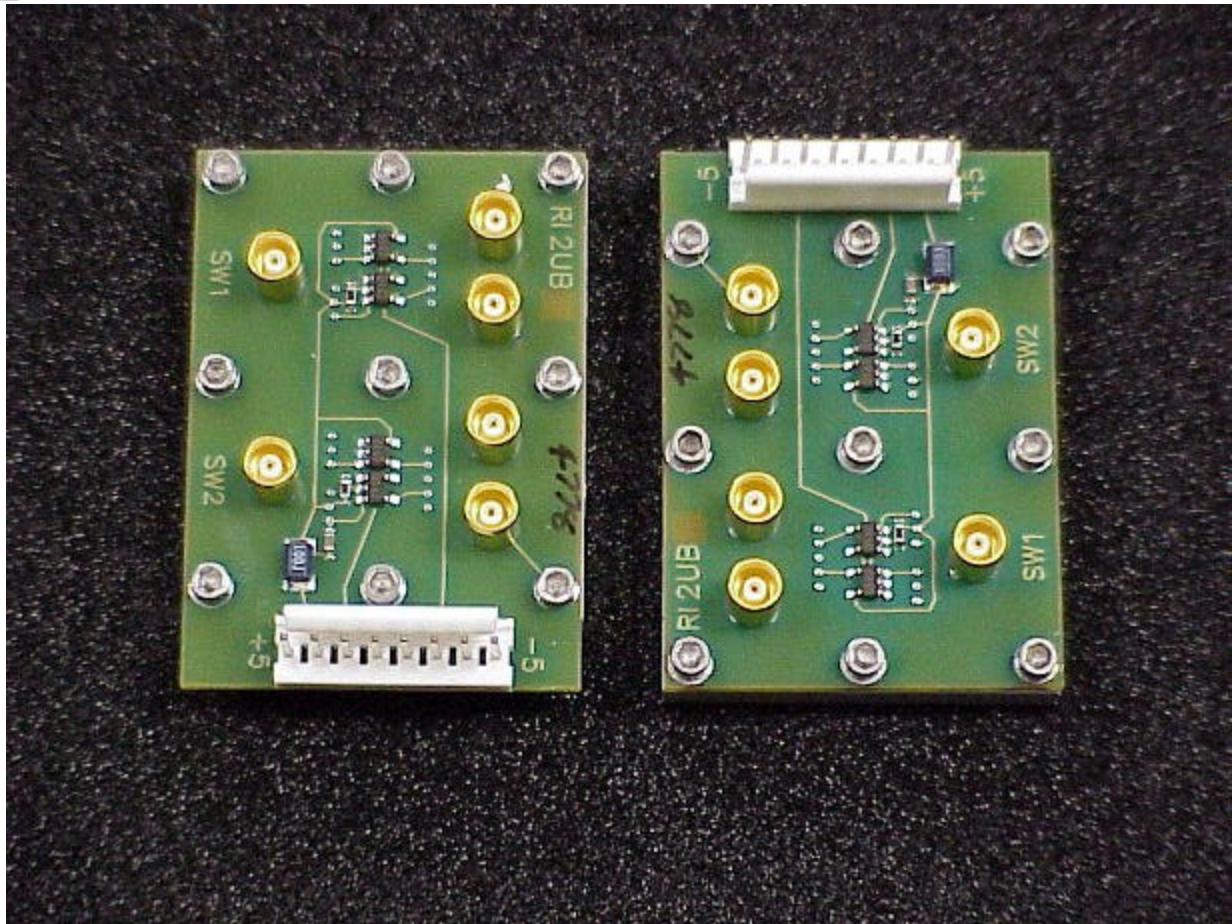


Figure 8
Picture

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RiK0015A I/O Buffer Single-ended Voltage Input to Differential Current Output Configuration

Revised: 04/03/2000 - 03/04/2002

Topic(s): Fixture

Doc ID:RBEH-4MERB7

RiK0015A

Single Ended Voltage to Differential Current Converter

Input: Voltage, Single-ended

	<u>Coax</u>
In-phase Voltage Input (I)	J4
Quadrature Voltage Input (Q)	J1

Output: Current, Differential

	<u>Header Pin</u>
In-phase, Positive Output (Ipos):	H1-1
In-phase, Negative Output (Ineg):	H1-2
Quadrature, Positive Output (Qpos):	H1-6
Quadrature, Negative Output (Qneg):	H1-5
Ipos, V to I Conversion	Vin / R3
Ineg, V to I Conversion	Vin / R4
Qpos, V to I Conversion	Vin / R1
Qneg, V to I Conversion	Vin / R2

<u>Component Identifier</u>	<u>Value</u>	<u>Size</u>
R1, R2, R3, R4 (Default Condition: divide by 2000)	2,000 Ohm	0603

Changes Required to Convert Module

	<u>Value</u>	<u>Size</u>
Check R11 to be loaded to 0ohm	0 Ohm	0603



RiK0015A I/O Buffer User Views and Configurations

Revised: 03/31/2000 - 10/29/2002

Topic(s): Fixture

Doc ID:RBEH-4MERB6

Document purpose:

To give to the user a physical view of the I/O buffer board as an aid in the process of configuring it for its various uses. Refer to the links listed below to see the specific configurations available for the module.

RiK0015A Differential I/O Buffer Module

The RiK0015A Differential I/O Buffer Module is a configurable, multi-purpose circuit for the manipulation of video frequency signals. It can be configured to buffer between any combination of single ended or differential I/O, voltage or current drive, at a user specified gain.

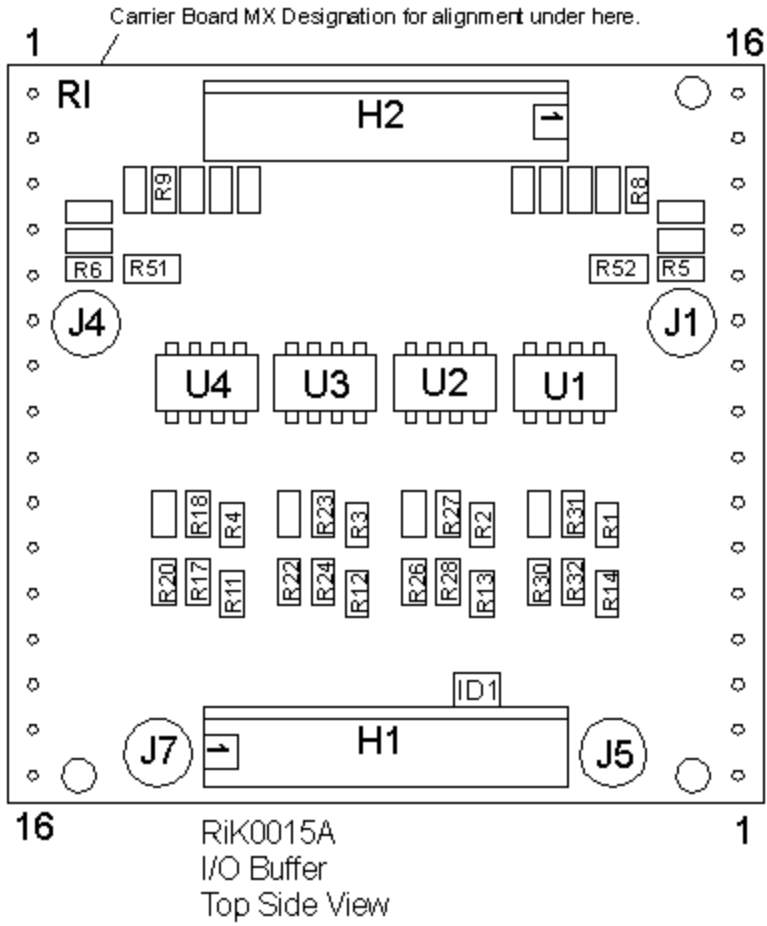
The various circuit configurations are established by the addition or removal of specified circuit resistors. The gain of the circuit is chosen by the selection of appropriate resistor values. See the specific configuration documentation for the gain resistor formulations. The default circuit is configured for single ended voltage input to differential **current** output with a gain of 1/2000 (ie. 1V in = 0.5 mA out).

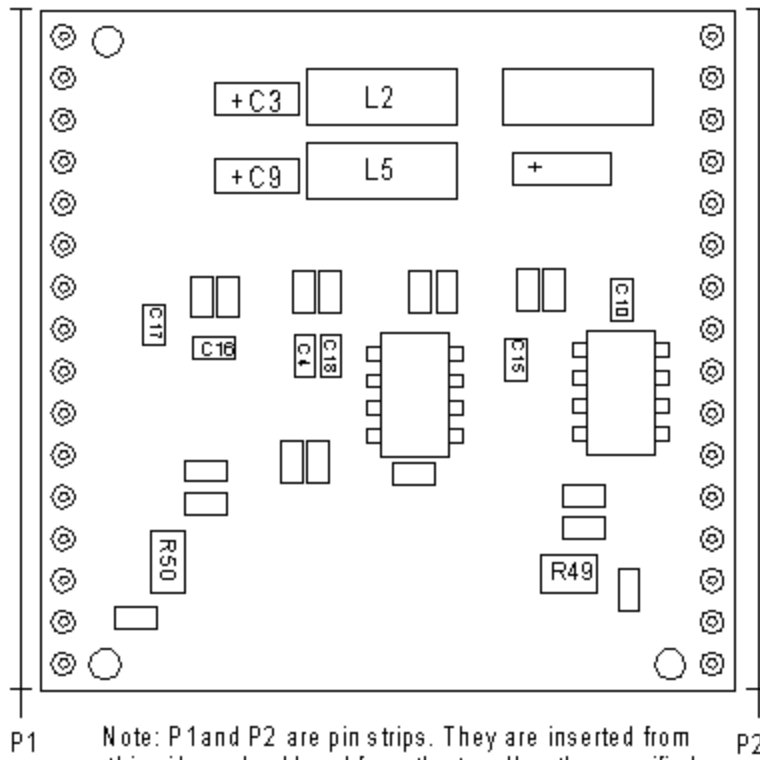
The circuit is designed to work in the RiK fixture. It is attached to the carrier board (typically in location M 1 or M2), which is mounted to the fixture top plate. The required +/- 15 voltages are provided through carrier board by the RiK fixture ribbon cables. The letters "RI" appear on the module to denote pin 1 and should be aligned with the "MX" (where x is the carrier board module location number ie: M1, M2 etc.) next to pin 1 on every available location on the carrier board (see module Top Side View below). Be careful to install the module in the correct orientation. The coaxial connectors are MCX female.

Configurations:

1. Single Ended Voltage Input to Differential Voltage Output.
2. Single Ended Voltage Input to Differential Current Output.
3. Differential Voltage to Single Ended Voltage Converter.

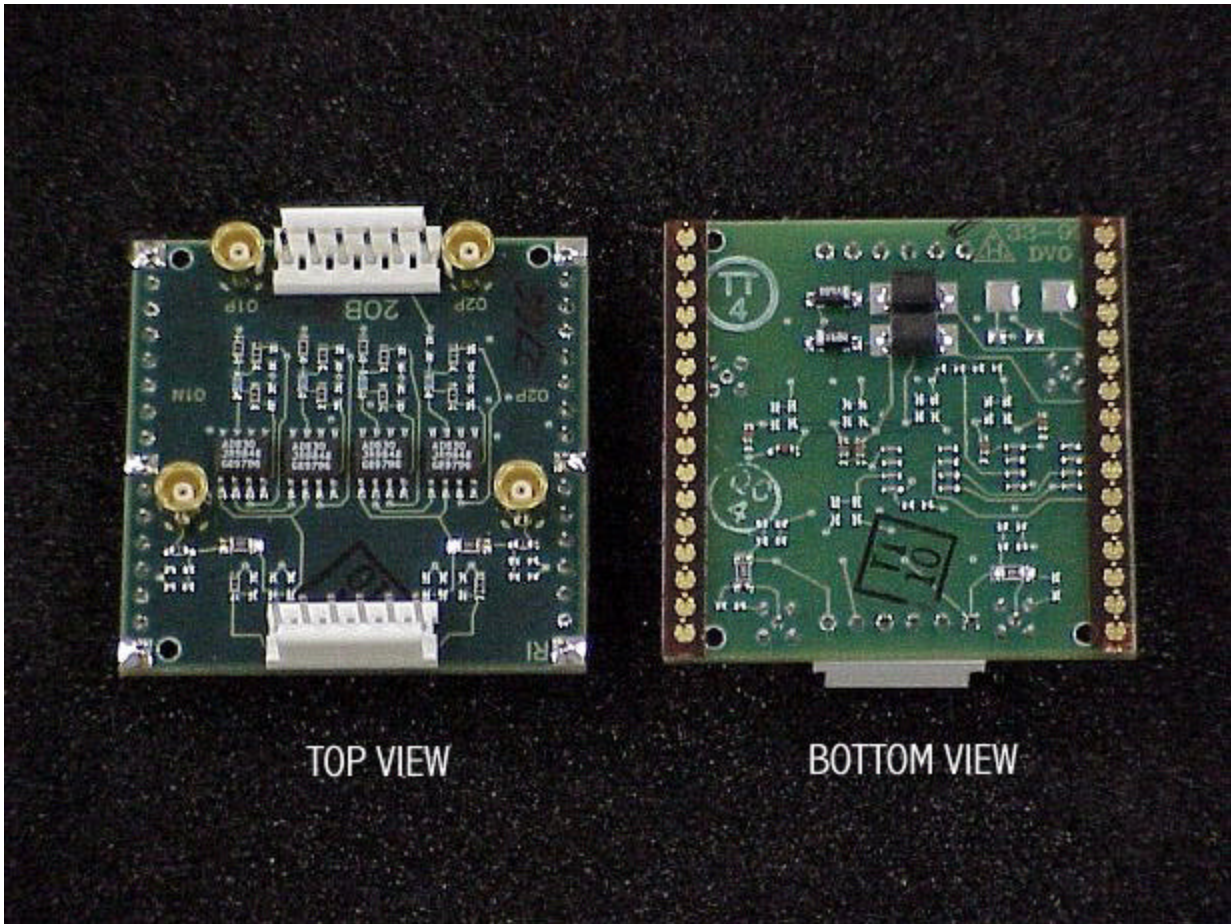






Note: P1 and P2 are pin strips. They are inserted from this side and soldered from the top. Use the specified fixture to align them during soldering.

RIK0015A
I/O Buffer
Bottom View



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RiK0015A I/O Buffer Single-ended Voltage to Differential Voltage Out Configuration

Revised: 03/20/2000 - 10/22/2002

Topic(s): Fixture

Doc ID:RBEH-4MERB5

RiK0015A

Single Ended Voltage to Differential Voltage Converter

Input: Voltage, Single-ended

	<u>Coax</u>
In-phase Voltage Input (I)	J4
Quadrature Voltage Input (Q)	J1

Output: Voltage Differential

	<u>Header Pin</u>
In-phase, Positive Output (Ipos)	H1-1
In-phase, Negative Output (Ineg)	H1-2
Quadrature, Positive Output (Qpos)	H1-6
Quadrature, Negative Output (Qneg)	H1-5
Ipos, V to V Conversion	1:1
Ineg, V to V Conversion	1:1
Qpos, V to V Conversion	1:1
Qneg, V to V Conversion	1:1

Changes required to convert module

Change the following Resistors

<u>Component Identifier</u>	<u>From Value</u>	<u>To Value</u>	<u>Size</u>
R1, R2, R3, R4	2000ohm	0 ohm	0603

Add the following Components:

<u>Component Identifier</u>	<u>Value</u>	<u>Size</u>
R20, R22, R26, R30	0 ohm	0603
Check R11 to be loaded to 0ohm		

Remove the following Components:

<u>Component Identifier</u>
R17, R24, R28, R32, R49, R50



RiK0015A Differential Voltage to Single-ended Voltage Converter Configuration

Revised: 04/03/2000 - 03/04/2002

Doc ID: RBEH-4MERB8

RiK0015A Differential Voltage to Single-ended Voltage Converter

Input: Voltage, Differential

	<u>Header Pin</u>
In-phase, Positive Input (Ipos):	H2-6
In-phase, Negative Input (Ineg):	H2-5
Quadrature, Positive Input (Qpos):	H2-1
Quadrature, Negative Input (Qneg):	H2-2

Output: Voltage, Single-ended

	<u>Coax</u>
In-phase Voltage Output (I)	J7
Quadrature Voltage Output (Q)	J5
I Signal Path Attenuation in dB	$20 \times \text{Log} (R24 / ((R24+R3)x2))$
Q Signal Path Attenuation in dB	$20 \times \text{Log} (R32 / ((R32+R1)x2))$

Changes Required to Convert Module

Change the following Components:
(For 30 dB attenuation)

<u>Component Identifier</u>	<u>Value</u>	<u>Size</u>
R20, R22, R26, R30	0 Ohm	0603
R24, R32	10 Ohm	0603
R12, R14	51.1 Ohm	0603
R1, R3	150 Ohm	0603

Remove the following components:

<u>Component Identifier</u>	
R8, R9, R11, R13, R17, R28	Remove these items



RIK0015A I/O Buffer - Providing a DC Offset to Output

Revised: 09/14/2000 - 10/22/2002

Topic(s): Fixture

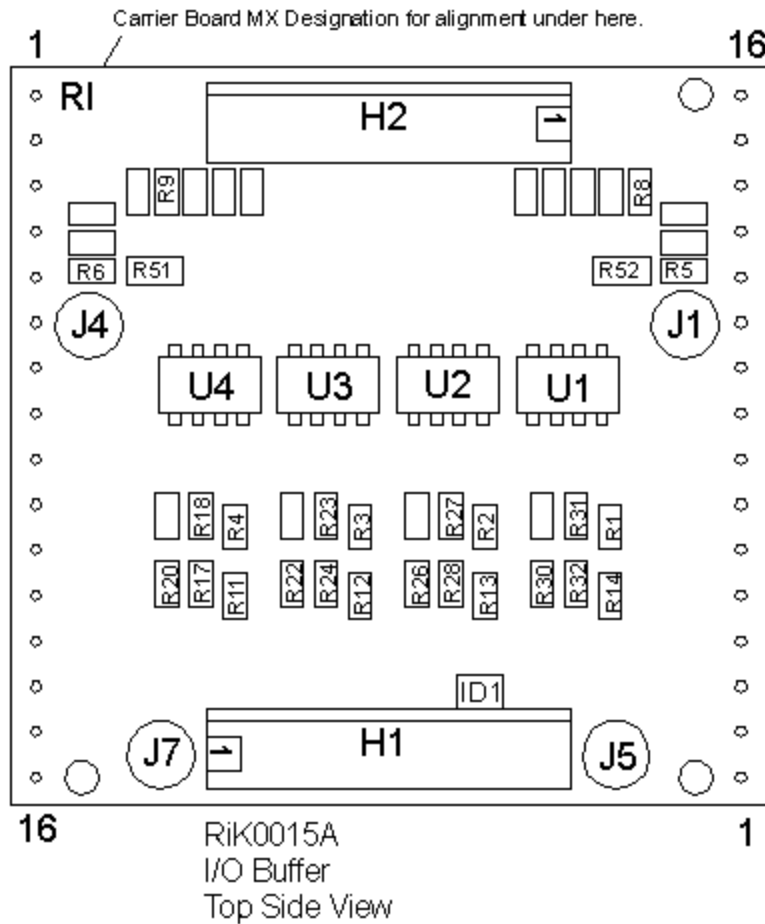
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Document Purpose:

It becomes necessary at times to provide a DC Offset to the Differential output of the Differential I/O module. The following procedure will describe how this can be done without providing an external board to do this .

Steps:

1. Configure the module for the Single Ended Voltage in / Differential Voltage Out configuration omitting the installation of R20, R22, R26, and R30. (see: [RIK0015A I/O Buffer Single-ended Voltage to Differential Voltage Out Configuration](#))
2. Strip and pre-tin one side of a 8" jumper wire for each intended power supply to be used in controlling the offset voltages.
3. Solder the jumper wire ends to the pin 3 side of U1, U2, U3, and U4. The easiest places to do this are at the pad sites intended for R20, R22, R26, and R30.
4. The actual offsets are controlled by the voltage applied to pin 3 of U1, U2, U3, and U4. Connect the other side of the 8" jumper wire to the DP pin intended for offset control.



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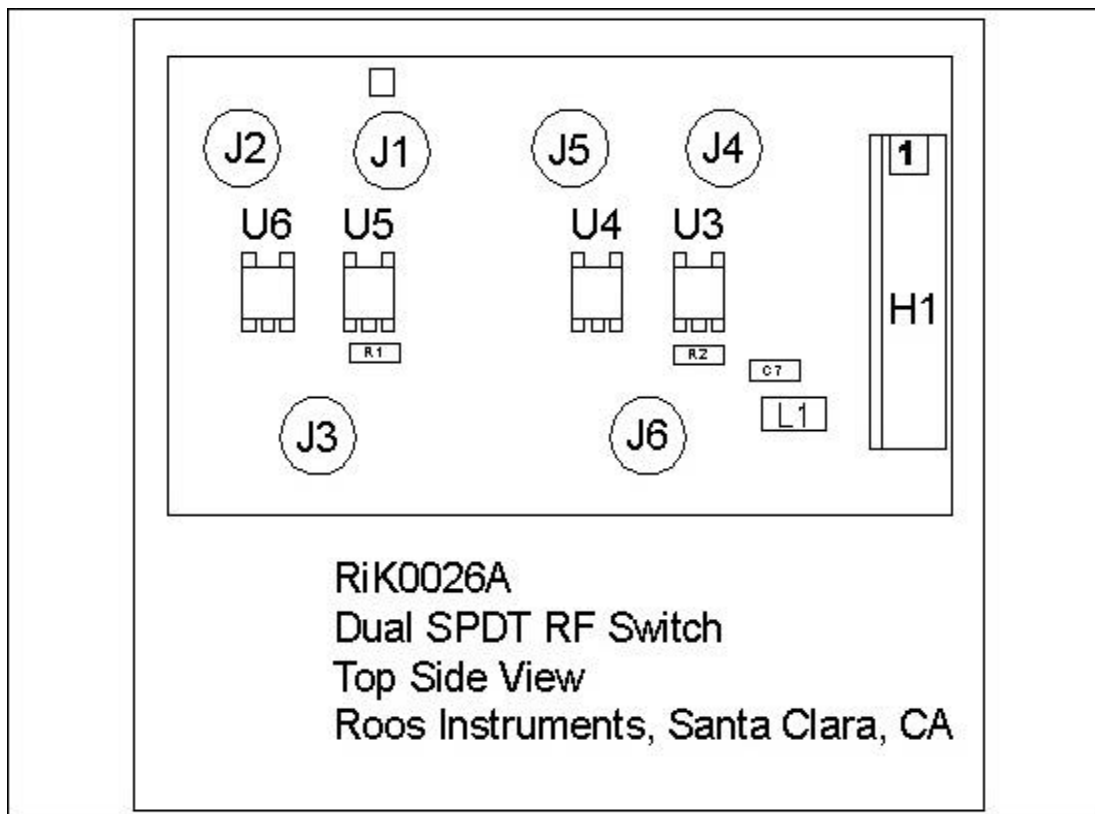
RIK0026B

Two, Dual SPDT RF Switch Modules

The RIK0026B Kit consists of two, dual SPDT RF switch modules, for a total of four SPDT switches. The switches are attached in the test fixture by standard 3M double sided adhesive tape.

Figures / Tables:

- [Figure 1](#) : Physical representation of the Switch Top Side view.
- [Table 1](#) : Pin Out
- [Table 2](#) : Typical Performance
- [Figure 2](#) : RF Default Conditions
- [Figure 3](#) : Insertion Loss Measurement.
- [Figure 4](#) : Isolation Measurement / Active to Inactive Port.
- [Figure 5](#) : Isolation Measurement / Common to Inactive Port.
- [Figure 6](#) : Common Port Return Loss
- [Figure 7](#) : Active Port Return Loss
- [Figure 8](#) : Picture



RIK0026B SPDT Switch Pin Out

Description	Connection	Type	Notes
+5V Supply	H1-8	Header Pin	
-5V Supply	H1-1	Header Pin	
Switch 1 Control	H1-3	Header Pin	
Switch 2 Control	H1-6	Header Pin	
Ground	H1-4/5		
Switch 1, Pole	J3	MCX Female	Not DC Blocked
Switch 1, NC	J1	MCX Female	Not DC Blocked
Switch 1, NO	J2	MCX Female	Not DC Blocked
Switch 2, Pole	J6	MCX Female	Not DC Blocked
Switch 2, NC	J4	MCX Female	Not DC Blocked
Switch 2, NO	J5	MCX Female	Not DC Blocked

Table 1
Pin Out**Switch 1 & 2 Typical Performance**

Current Drain +/-5V ALL CBITS HI	100uA Max
Current Drain +/-5V 1 CBIT LOW	500uA typical
Current Drain +/-5V 2 CBITS LOW	1mA typical
Insertion Loss (Activated)	Fig. 3
Minimum Freq.	DC
Max Freq.	6GHz
Isolation / NC to NO	Fig. 4
Isolation / Pole To Inactive	Fig. 5
Common Port Return Loss	Fig.6
Active Port Return Loss	Fig.7
2nd Harm @13dBm Pin 880MHz	60dBc
3rd Harm @13dBm Pin 880MHz	65dBc

Table 2
Typical Performance



Figure 3
Insertion Loss

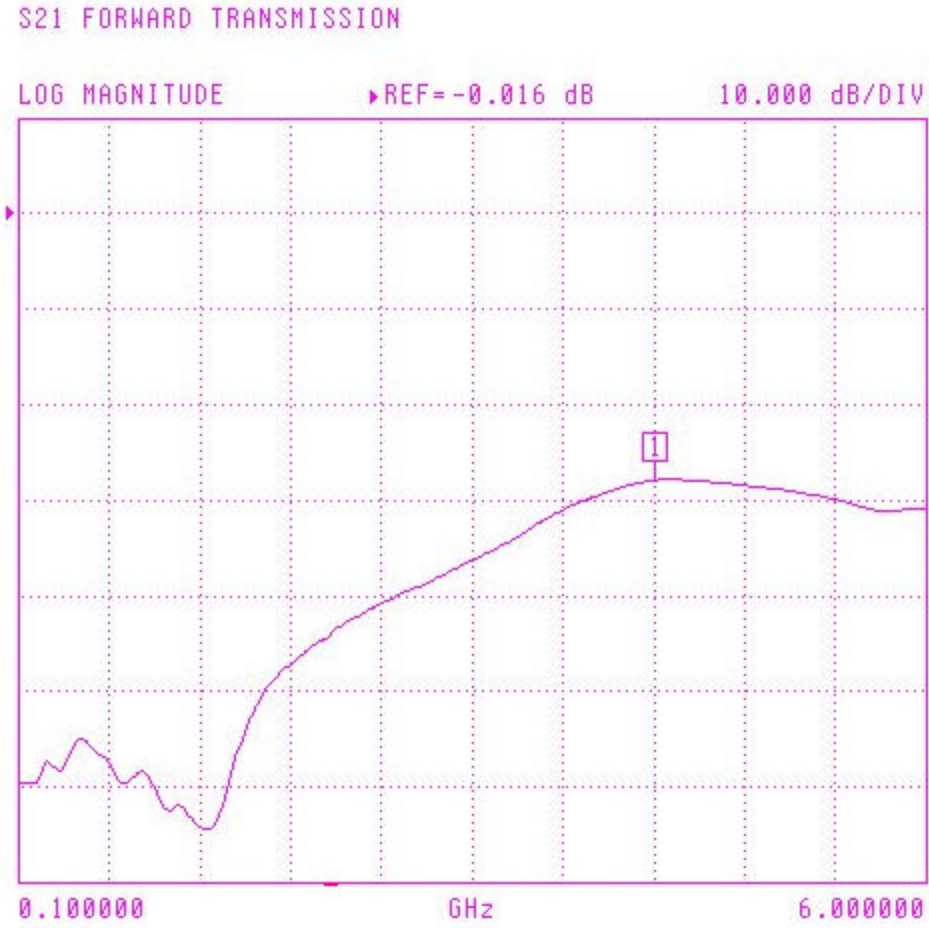


Figure 4
Isolation NO to NC Port

S21 FORWARD TRANSMISSION

LOG MAGNITUDE

REF = -0.016 dB

10.000 dB/DIV



Figure 5
Isolation Common to Inactive Port

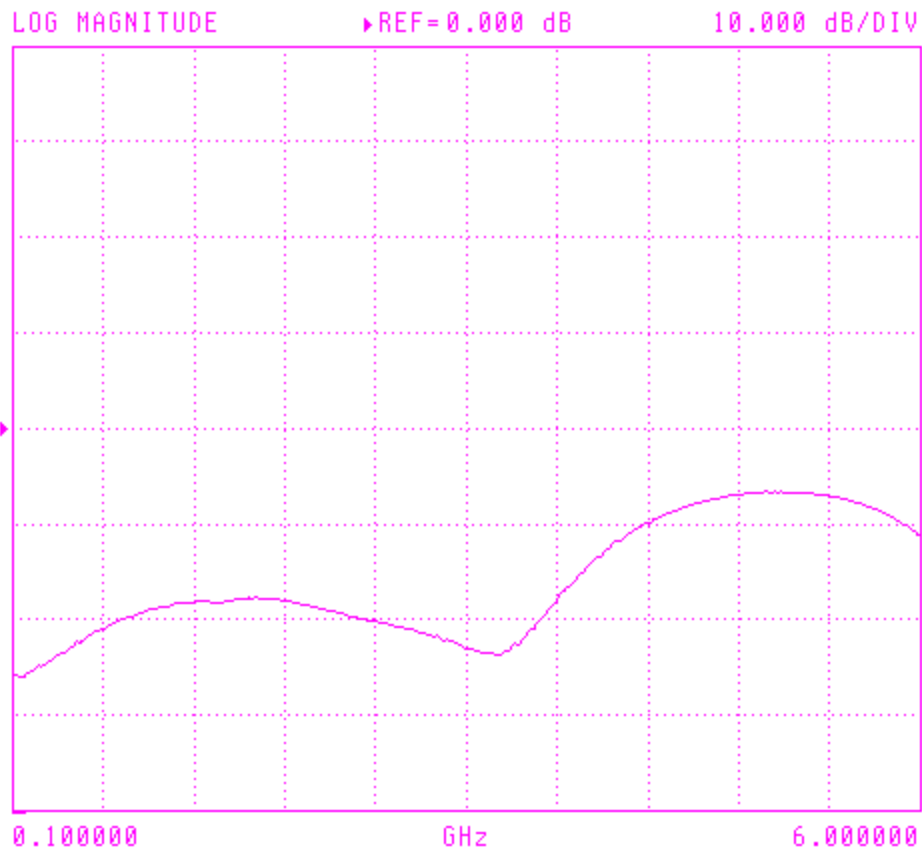


Figure 6
Common Port Return Loss

S22 REVERSE REFLECTION

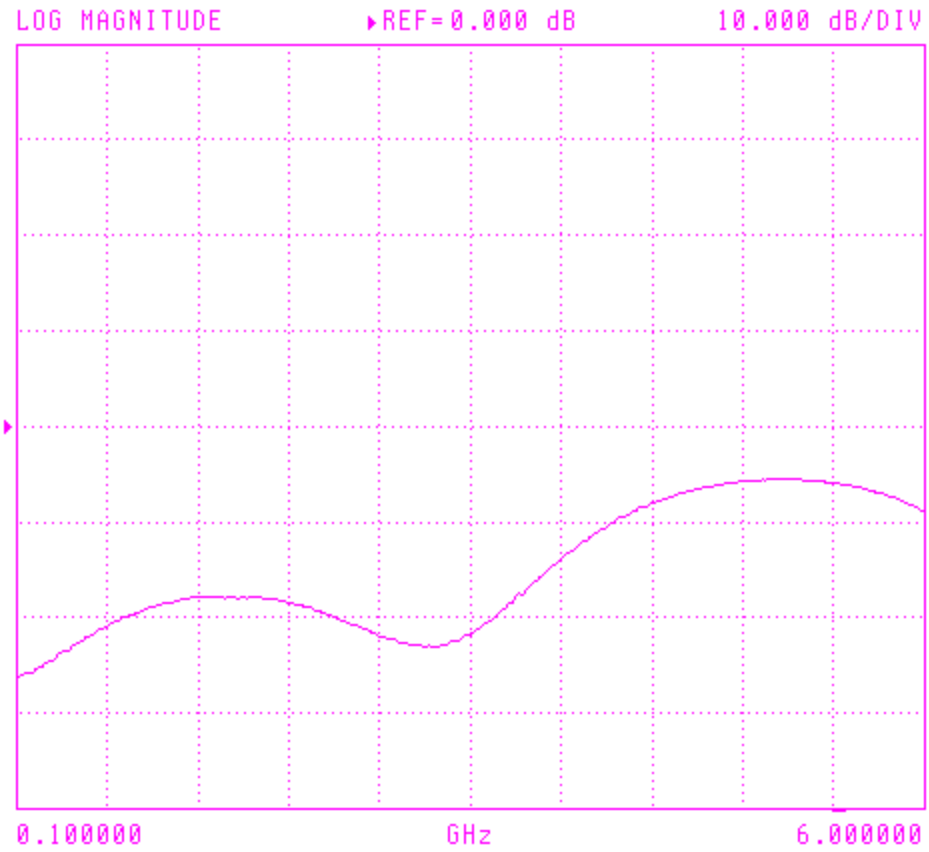


Figure 7
Active Port Return Loss

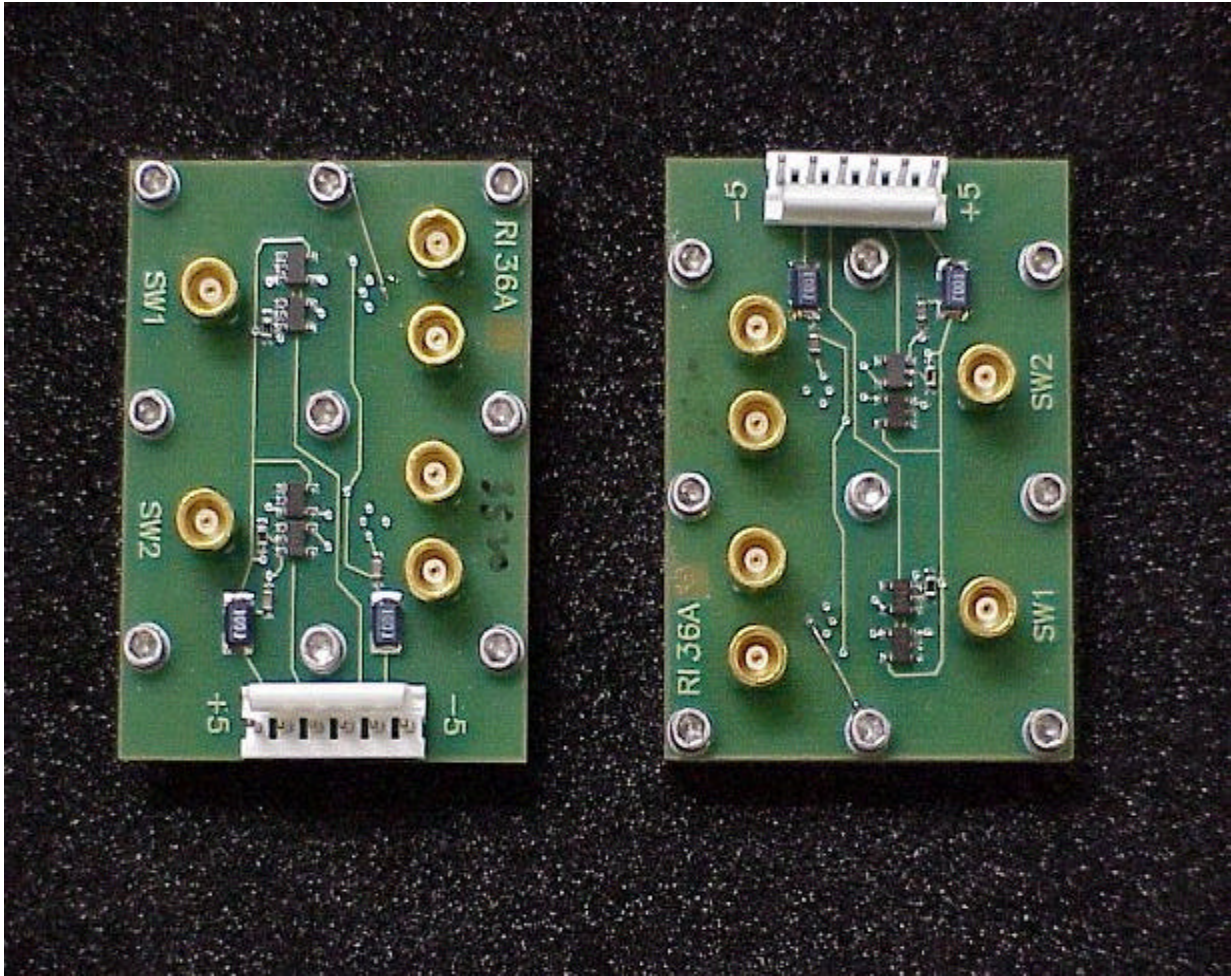
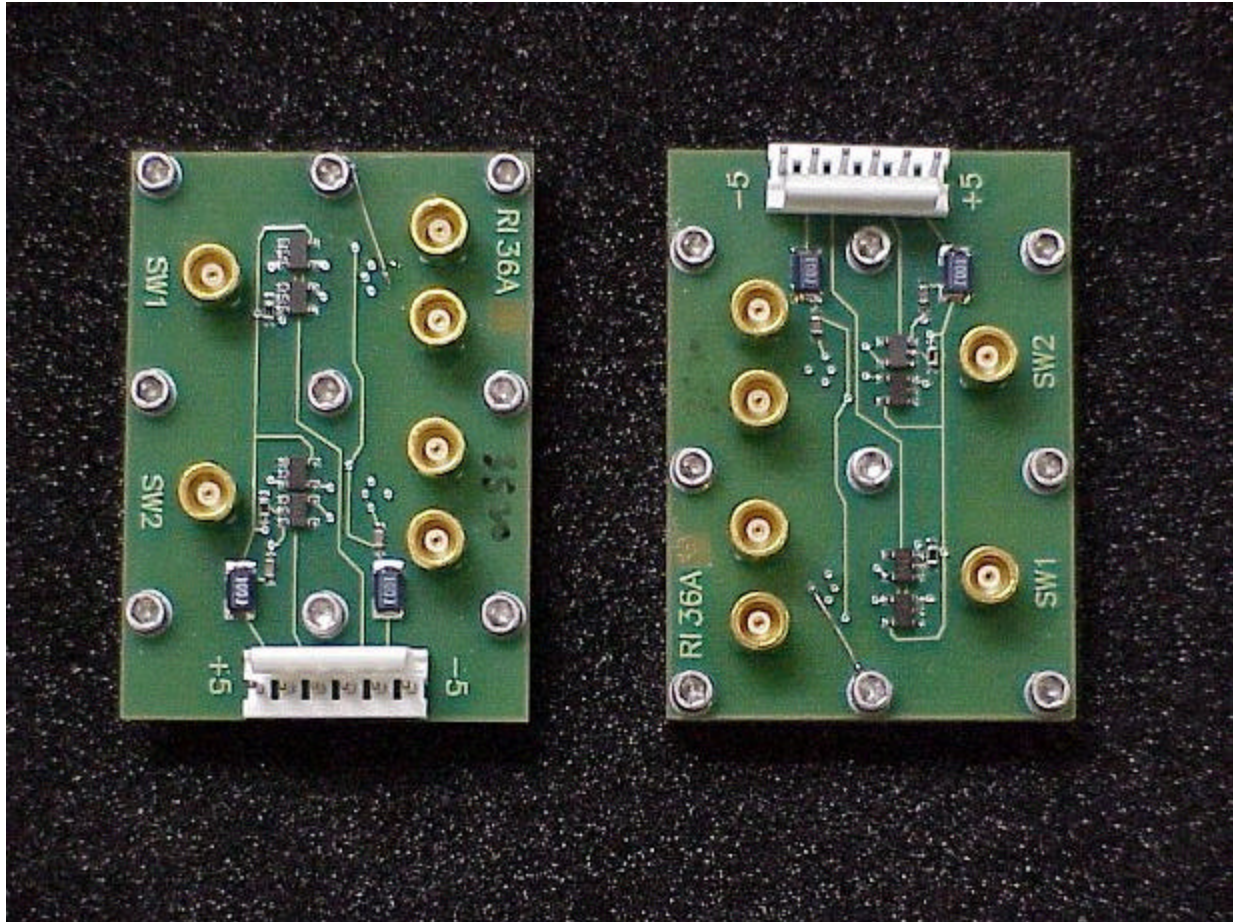


Figure 8
Picture

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RIK0026B, DUAL SPDT SWITCH PICTURE



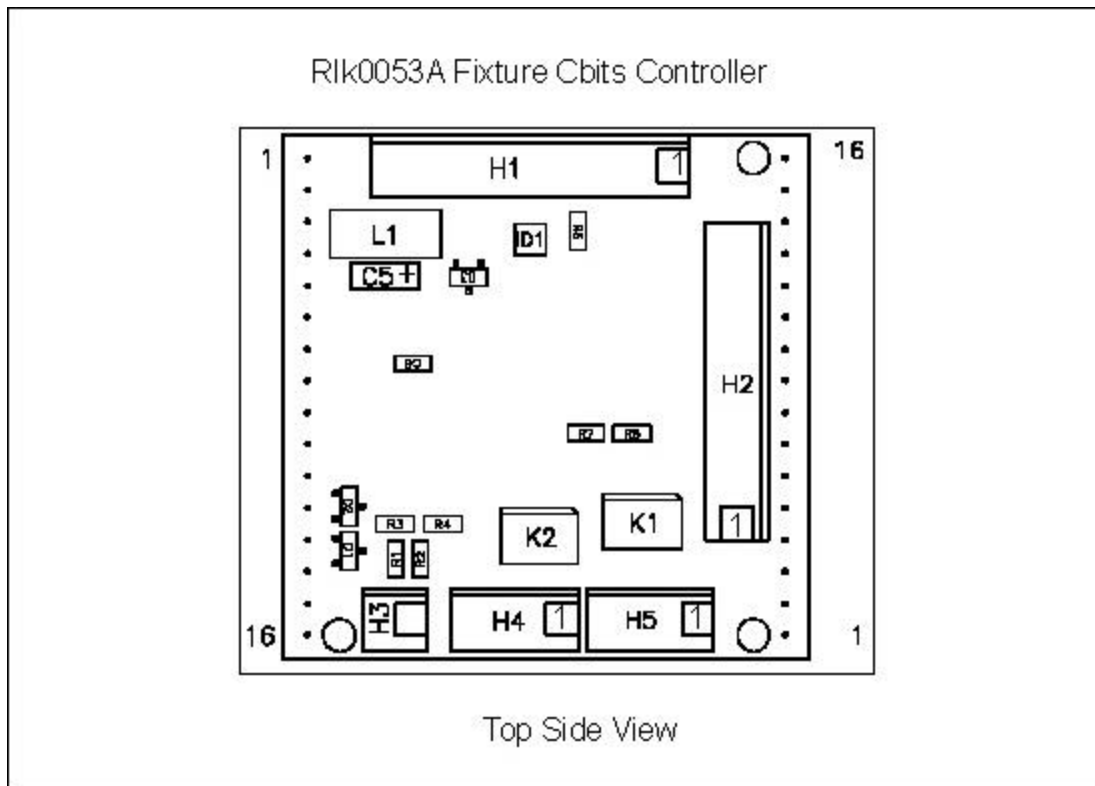
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Purpose: To describe the RIK0053A Fixture Cbit Controller and its use.

The standard fixture control circuitry includes eight Cbits that can be used to control or drive devices needed to route or otherwise process signals to the DUT. In some instances more than eight are required. It is for this reason that ROOS Instruments developed the RIK0053A Fixture Cbit Controller. The following is a description with programming notes of this fixture module.

Top View:



Pin Out:

Header #	Pin #	Function
1	1	Cbit 8
1	2	Drive voltage
1	3	Cbit 7
1	4	Drive voltage
1	5	Cbit 6
1	6	Drive voltage
1	7	Cbit 5
1	8	Drive voltage
1	9	Drive Voltage Input
1	10	Gnd Connect
2	1	Cbit 1
2	2	Drive voltage
2	3	Cbit 2
2	4	Drive voltage
2	5	Cbit 3
2	6	Drive voltage
2	7	Cbit 4
2	8	Drive voltage
2	9	Drive Voltage Input
2	10	Gnd Connect

Note:

Pins 2,4,6,8, and 9 on headers 1&2 are common.

Fixture requirements:

1. Smart Carrier (RIK0014A).
2. Press in connector strips (16 pin) installed at desired module locations (M1 - M16).

Cbits Available:

1. First three standard Cbits as found on the fixture carrier (Cbit 1 - 3).
2. Eight open collector Cbits per Switch Driver Module plus two optical Cbits.

Coding Requirements:

Fixture Carrier Position#	Smart Carrier Module#
M1	M1
M2	M2
M3	M3
M4	M4
M13	M5
M14	M6
M15	M7
M16	M8

1. When writing to a standard Cbit (found on the fixture carrier board) the format is of **CXY**
 C = C, X = control bit used (only 1-3 are usable on the smart carrier), Y = 1 or 0.

Ex. C20 Sets the standard Cbit#2 low.

2. When writing to a Smart Carrier Cbit Module the format is of **M#AXXXXXXXX**. M = M, # = Module number being written to, A = A, X = 1, X, or 0.

Ex. M4XXXXXXXX1X Writes to Smart Module #4 and sets bit#2 low.

3. When combining standard Cbit commands and Smart Module commands place the standard commands first.

Ex. C10M4A001110XX Sets standard Cbit#1 low. It then writes to Smart Module #4 and sets the appropriate Cbits for the 70dB setting on the attenuator.

4. When combining to Smart Module commands combine them in one long string.

Ex. M4XXXXXXXX1M8A001110XX0 Writes to module #4 and sets its bit#1 low. It then writes to module #8 and sets its bit#1 high

5. When using the Smart Carrier Cbit Module to control a programmable attenuator **ALL** bits associated with the attenuator need to be driven either high or low.

Ex. M8A001110XX Writes to Smart Module #8 and controls Cbits 8-3 to set the atten to 70dB.

Note: Observe that the 1 = High on a standard Cbit while 1 = Low on a Smart Module Cbit.

Opto Cbits Programming:

1. When writing to a Smart Carrier Opto Cbit the format is of **S#1XX1**
S = S, # = Module number being written to, X = 1, X, or 0.
0 = closed (0V) and 1 = open (3.8V)
Bit position = S# DS1 DS2 DS3 DS4

Software Fixture Considerations:

1. When creating the software fixture ALL Cbits should be given a default state other than "X". Define these states on the first path entry of the software fixture.

Ex. DutRf2 Rf2 default M4A00000011M8A00000011.

Note: If this is not done then it is possible that an error will occur and appear in the programmer message window.

"Error undefined bit in fixture module M4 value 0000001X"

The X defines in this case the Cbit that needs a default state.

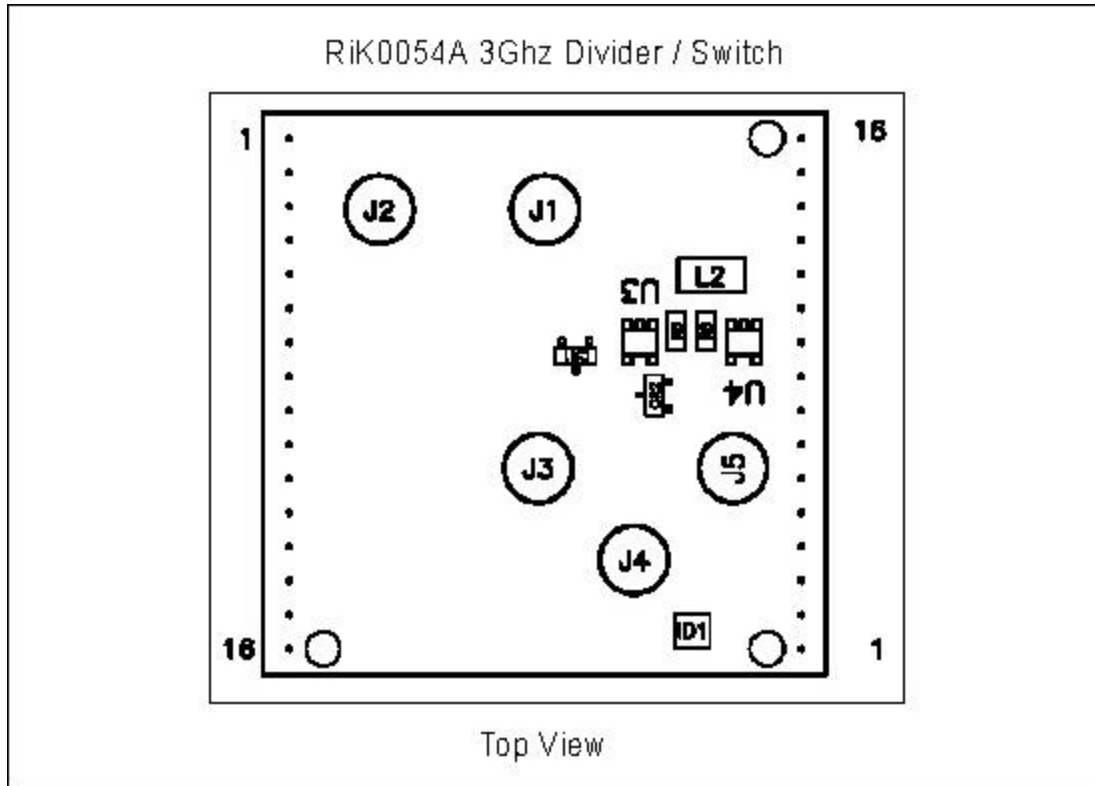


RIK0054A - 3GHz Divider / SPDT Switch

Purpose: To describe the RIK0054A 3GHz Divider with SPDT switch and its use.

The RIK0054A is a dual function Module. It incorporates a 3GHz frequency divider (64/128/256) and an independent 3GHz SPDT non-reflective switch.

Top View:



Fixture requirements:

1. Smart Carrier (RIK0014A).
2. Press in connector strips (16 pin) installed at desired module locations (M1 - M16).

Coding Requirements:

Fixture Carrier Position#	Smart Carrier Module#
M1	M1
M2	M2
M3	M3
M4	M4
M13	M5
M14	M6
M15	M7
M16	M8

PIN#	Function	Notes:																								
J1	Divider Input	Max Power in = 10dBm, fin(lower typical) = 40Mhz @ 6dBm in.																								
J2	Divider Output	<p>Square wave, divider ratio is statically set by 0 ohm resitors to ground or +5V, DS1-DS3 are not to be controlled by the Smart Carrier.</p> <p>Divider Truth Table</p> <table border="1"> <thead> <tr> <th></th> <th>Enabled</th> <th>Disabled</th> <th>fin/256</th> <th>fin/128</th> <th>fin/64</th> </tr> </thead> <tbody> <tr> <td>DS1</td> <td>0</td> <td>1</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>DS2</td> <td>X</td> <td>X</td> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>DS3</td> <td>X</td> <td>X</td> <td>0</td> <td>1</td> <td>1</td> </tr> </tbody> </table>		Enabled	Disabled	fin/256	fin/128	fin/64	DS1	0	1	0	0	0	DS2	X	X	0	0	1	DS3	X	X	0	1	1
	Enabled	Disabled	fin/256	fin/128	fin/64																					
DS1	0	1	0	0	0																					
DS2	X	X	0	0	1																					
DS3	X	X	0	1	1																					
J3	Switch output NO	S#XXX0																								
J4	Switch input	Max input +24dBm, input 1dB comp typical = 21dBm																								
J5	Switch output NC	S#XXX1																								

Divider Rf Performance:

Single Tone Performance

Pin (dBm)	Freq Low	Freq High
6	<100 MHz	3 GHz
-15	<400 MHz	3 GHz
-20	<500 MHz	3 GHz

Two Tone Performance (defined by the dividers ability to accurately measure the freq of the strongest signal)

Pin Fund (dBm)	Pin 2nd (dBm)	Delta Freq (MHz)	Freq Low (MHz)	Freq High (MHz)
+6	+5	1	<200	3000
0	-1	1	<200	3000
0	-2	2	<200	3000
-5	-8	2	<200	3000

Basically the less power available the larger the delta power or larger the freq offset needed. The best low power performance occurs at the high end of the frequency band.

RF SPDT Switch Control Programming:

1. When writing to a Smart Carrier Cbit the format is of **S#XXXX**
S = S, # = Module number being written to, X = 1, X, or 0.
0 = closed (0V) and 1 = open (3.8V)
Bit position = S# DS1 DS2 DS3 DS4

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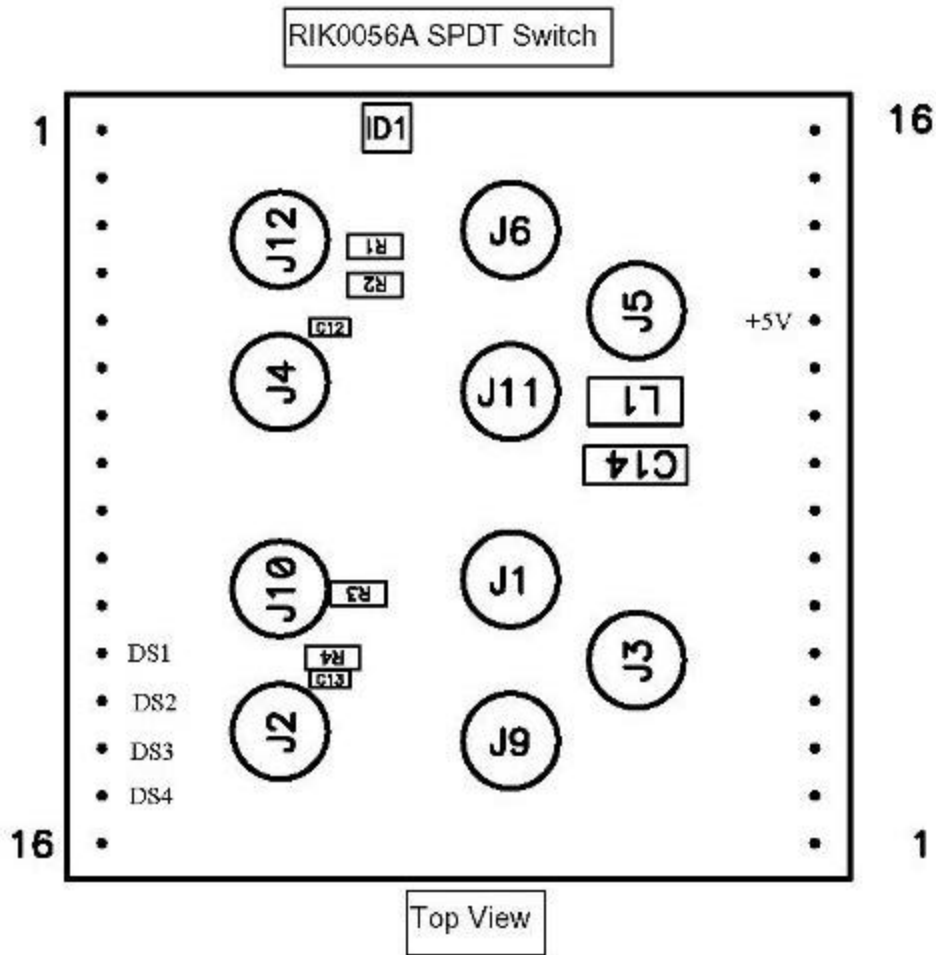
RIK0056A SP4T RF Switch

Revised: 01/28/2003 - 03/14/2003

Topic(s): Fixture

Purpose - to describe the RIK0056A as a fixturing option and to provide information on its performance.

The RIK0056A includes one DUAL SP4T wide band (6 GHz) RF module. It is intended to be used with the RIK0014A smart carrier. It is especially easy to use since DC wiring is not required when used in conjunction with the smart carrier. It also helps to reduce fixture complexity where a high level RF of switching is required.



Pin Out:

Pin#	Function	DS1	DS2	DS3	DS4	Connector Type
P2:12	+5V					Header Pin
P2:11	-5V					Header Pin
P1:12	DS1					Header Pin
P1:13	DS2					Header Pin
P1:14	DS3					Header Pin
P1:15	DS4					Header Pin
P1:16	Grnd					Header Pin
J1	SW2 NO	X	X	0	0	MCX Female
J2	SW2 NO	X	X	0	1	MCX Female
J3	SW2 Common					MCX Female
J4	SW1 NO	0	1	X	X	MCX Female
J5	SW1 Common					MCX Female
J6	SW1 NO	0	0	X	X	MCX Female
J9	SW2 NC	X	X	1	1	MCX Female
J10	SW2 NO	X	X	1	0	MCX Female
J11	SW1 NC	1	1	X	X	MCX Female
J12	SW1 NO	1	0	X	X	MCX Female

Coding Requirements:

Fixture Carrier Position#	Smart Carrier Module#
M1	M1 (S1)
M2	M2 (S2)
M3	M3 (S3)
M4	M4 (S4)
M13	M5 (S5)
M14	M6 (S6)
M15	M7 (S7)
M16	M8 (S8)

Fixture requirements:

1. Smart Carrier (RIK0014A).
2. Press in connector strips (16 pin) installed at desired module locations (M1 - M16).

Cbits Programming:

1. When writing to a Smart Carrier Cbit the format is of **S#10X1**
 S = S, # = Module number being written to, X = 1, X, or 0.
 Bit position = S# DS1 DS2 DS3 DS4

Electrical Performance:

Maximum Ratings

Bias Voltage Range	+7.0 Vdc
Control Voltage Range	-0.5V to Vdd + 1V
Maximum Input Power	+16 dBm (0.05 - 0.5 FHz)
Vdd = +5 Vdc	+22 dBm (0.5 - 6.0 GHz)

Electrical Specifications

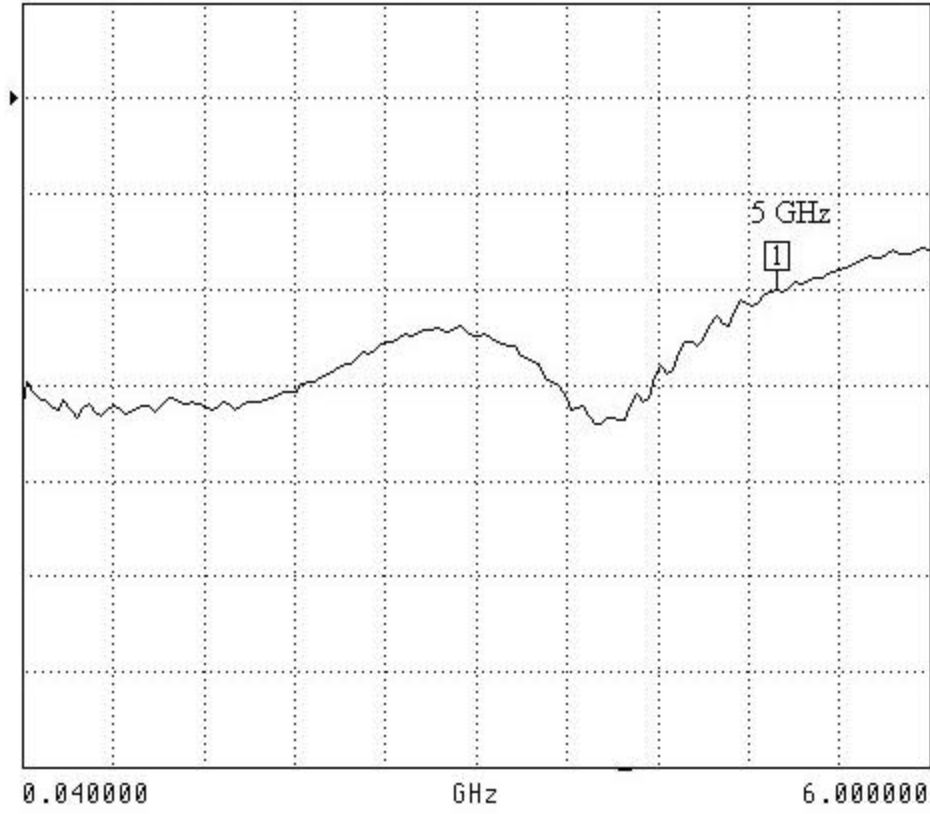
Parameter	Frequency	Min.	Typ.	Max.	Units
Vdd		4.5		5.5	V
Idd @ 5.0Vdc			3.0	5.0	mA
TTL/CMOS Control					
Low 0 to +0.8Vdc			5		uA
High +2.0 to +5.0 Vdc			50		uA
Insertion Loss	DC - 4.0 GHz		2.5		dB
	DC - 6.0 GHz		4.5		dB
Isolation	DC - 3.0 GHz		40		dB
	DC - 6.0 GHz		35		dB
Return Loss (Common)	DC - 5.0 GHz		12		dB
	DC - 6.0 GHz		7		dB
1dB Compression	0.5 - 6.0 GHz		20		dBm
IIP3 +7dBm each tone	0.5 - 6.0 GHz		43		dBm
Switching	0.5 - 6.0 GHz				
tRISE, tFALL (10%/90% RF)			35		nS
tON, tOFF (505 CTL to 10%/90% RF)			150		nS

S21 Forward Transmission



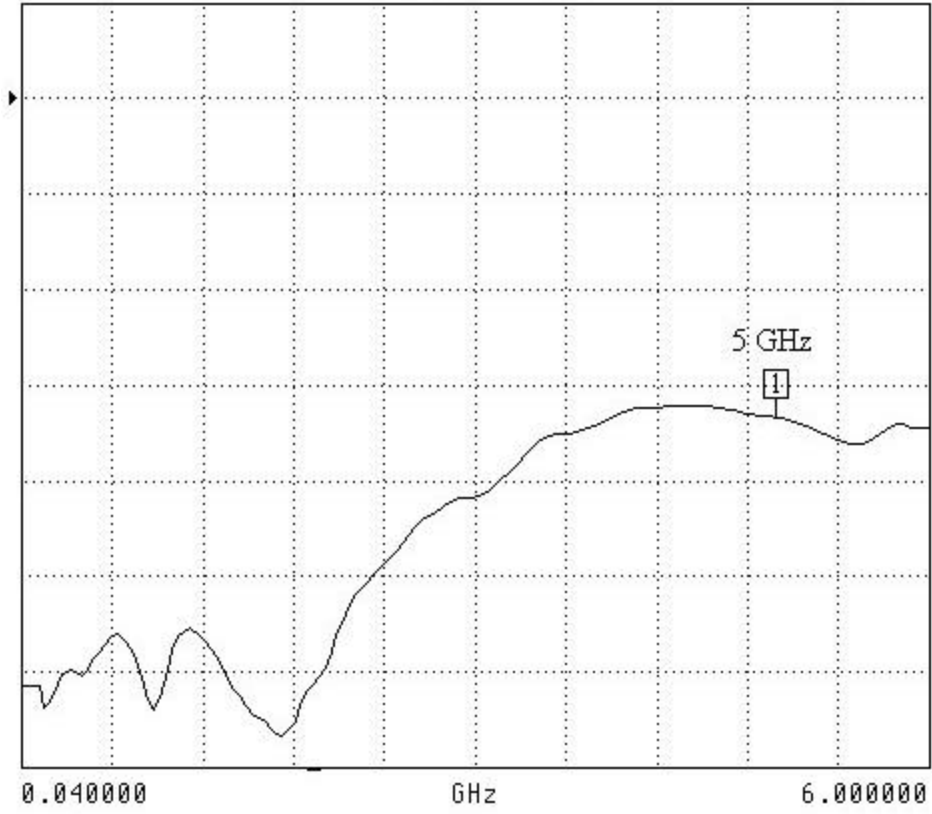
S11 Forward Reflection

LOG MAGNITUDE REF=0.000 dB 5.000 dB/DIV



From Normally Closed to Normally Open

LOG MAGNITUDE ▶ REF=0.000 dB 10.000 dB/DIV



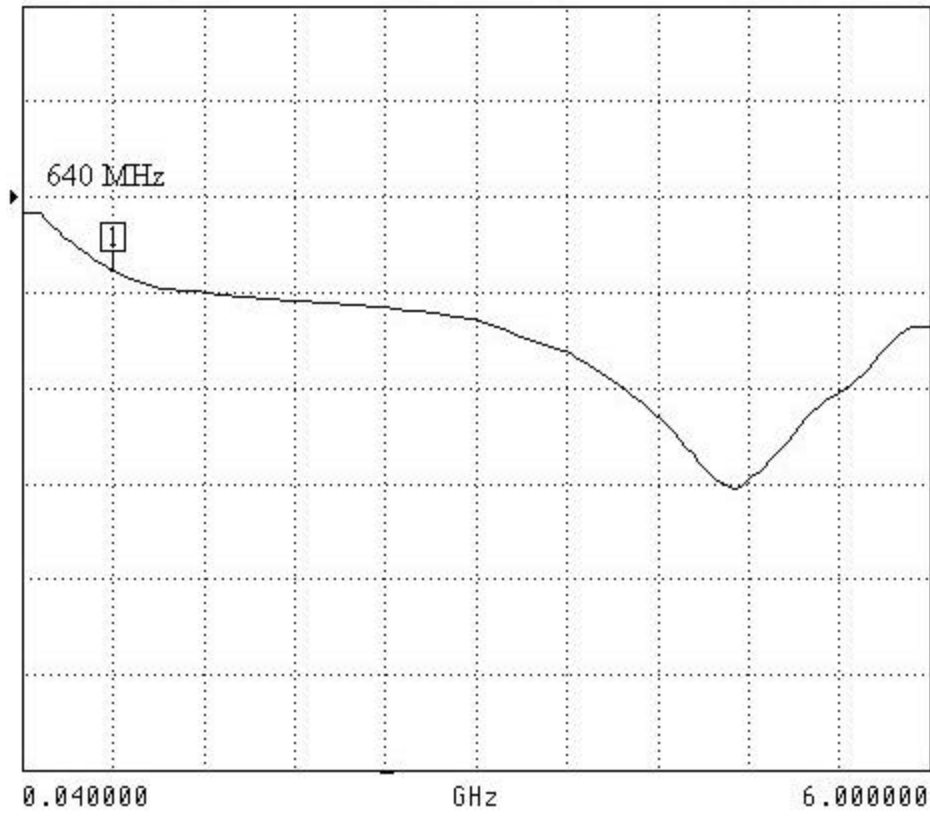
S11 Normal Open Open State

Fixturing - CH 2: Modules

LOG MAGNITUDE

REF=0.000 dB

10.000 dB/DIV



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Document Purpose:

To provide to the test engineer a guide for debugging a hardware fixture after repair or assembly.

Steps:

1. The fixture should be configured as shown in Figure 1. This allows easy access to the RF, static digital, and other pins attached to the DIB. Install it onto the test head and activate the software fixture.
2. Choose a test plan that will allow you to set a break point. A preferred selection would be one that is intended to be used with the fixture being debugged.
3. Compile the test plan and run it after setting a break point.
4. At the breakpoint use the tester controller to toggle and set voltages on the various pins associated with the fixture.
5. Verify that they are attached properly using a voltmeter attached to the specific pogo pins desired. You can also use the built in V measures on the tester. When doing this make sure that the DIB and DIB board clamp are not installed.

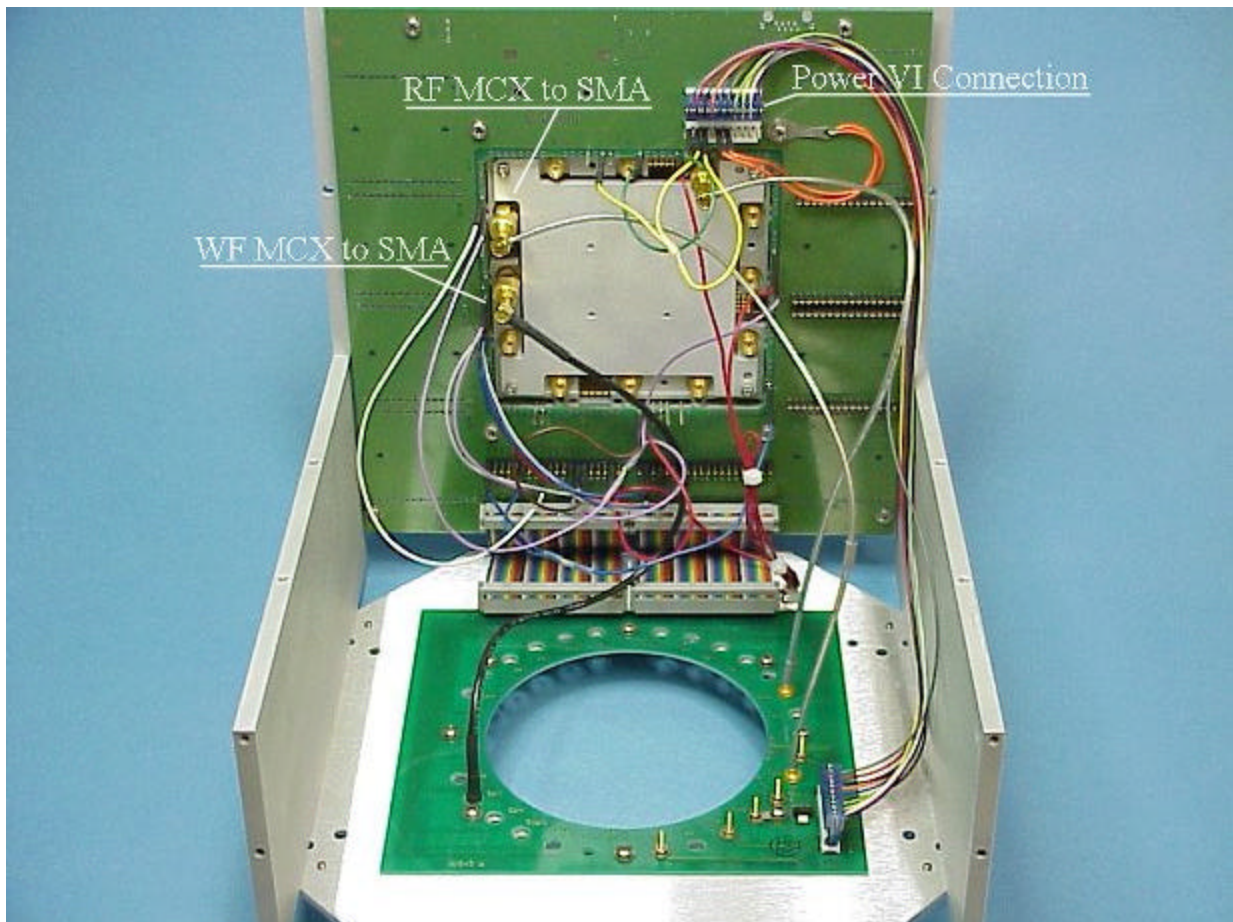


Figure 1.

Common Fixture Problems :

1. Unable to measure the set voltage on a particular pin. For example you may have set 5.0V but measure 5.1V.
 If the pin is attached to a VCC or Static Digital Pin.
 Suggestion: Make sure the ground reference (GNDREF) is connected to the desired ground.
 If the pin is attached to a Power VI.
 Suggestion: Make sure the VRTNS and RTNS pins are connected to the desired ground.

2. Unable to measure the set voltage on a particular pin. For example you may have set 5.0V but measure as if shorted.
 Suggestion: Make sure the DIB board clamp is not installed with out the DIB board itself. The clamp will short the pogo pins to ground.
 Suggestion: Make sure the pogo pin pad on the DIB is not shorted to ground.
 Suggestion: Check the pogo pin alignment to make sure that the pogo pin is not shorted to the fixture top plate.
 Suggestion: Make sure that DC blocks have been provided on the RF pins. A short on an RF pin can draw down a DC pin voltage.
 Suggestion: Make sure the fixture is seated and docked properly on the test head.
 Suggestion: Make sure of continuity between the test head and the carrier board pogo pin.
 If the pin is attached to a Power VI.
 Suggestion: Make sure the cable connections on the pin headers are installed and aligned properly.

3. Unable to measure with a Vmeasure pin. Pin acts as if shorted.
 Suggestion: Check Suggestions mentioned in 2.
 Suggestion: If the tester has an I_Drive capability (older tester) and the fixture is of new vintage then the I_Drive pin is being grounded by the fixture. Clip Pin#32 on header#1.

4. High path loss through a SPDT switch.
 Suggestion: Make sure that the fixture power is turned on.
 Suggestion: Make sure that +/-5V appears at the switch pin header (pin 1= -5V and pin 8 = +5V).
 Suggestion: Make sure the proper control bit (CBIT) is being controlled and is in the proper state.
 The normally closed position is active when the CBIT is high.

Fixture Warnings:

1. **Warning: Once the RF (SSIS to MCX) cables are installed allow them to launch from the pogo circuit board for 1 inch before bending. Bending them at the SSIS connector directly can result in connector damage both on the fixture and on the test head.**

















Document Purpose:

To provide the test engineer a guide in **Assembling a Hardware Fixture** to be used on the RI 7100A tester.

What does the Hardware Fixture do?

The hardware fixture provides a **Resource Interface** between the tester's **Test Head** and the **DUT Interface Board**.

Standard Fixturing Kits available through RI:

<u>Part Number</u>	<u>Description</u>	
RiK0001A	RF Cable Kit (SSIS to MCX, 6 cables)	
RiK0002A	WF Cable Kit (DIN to MCX, 5 cables)	
RiK0004A	Test Fixture Bottom Assembly Kit	
RiK0005A	RF Cable Kit (MCX to MCX, 5 cables)	
RiK0007A	DC Jumper Wire Kit (40 Jumper Wires)	
RiK0008A	SMA to MCX Adapters Kit (5 Adapters)	
RiK0009A	SMA to SSIS Adapters Kit (5 Adapters)	
RiK0012A	Test Fixture Top Plate Assembly (Requires RiK0013A or RiK0014A)	
RiK0013A	Passive Carrier Assembly Kit	
RiK0014A	Active Carrier Assembly Kit	
RiK0015A	Differential I/O Module Kit	
RiK0018A	Test Fixture Engineering Plate	
RiK0020A	Fixture Ramps (1 pr)	
RiK0021A	Fixture Ramps, Old (1 pr)	
RiK0026A	RF Switch Modules Kit 6GHz (4 SPDT RF Switches)	

Major Steps:

1. [Fixture Bottom Assembly](#)
2. [Top Plate Assembly](#)
3. [RF Cable Installation](#)
4. [Finishing the Assembly](#)

A) Fixture Bottom Assembly:

1. Install the two **fixture sides** as shown in Figure 1. Notice the **locking cam notch** orientation.
2. Install the two 40 conductor **ribbon cables** and the 10 conductor **power VI** cable as shown in [Figure 2](#).

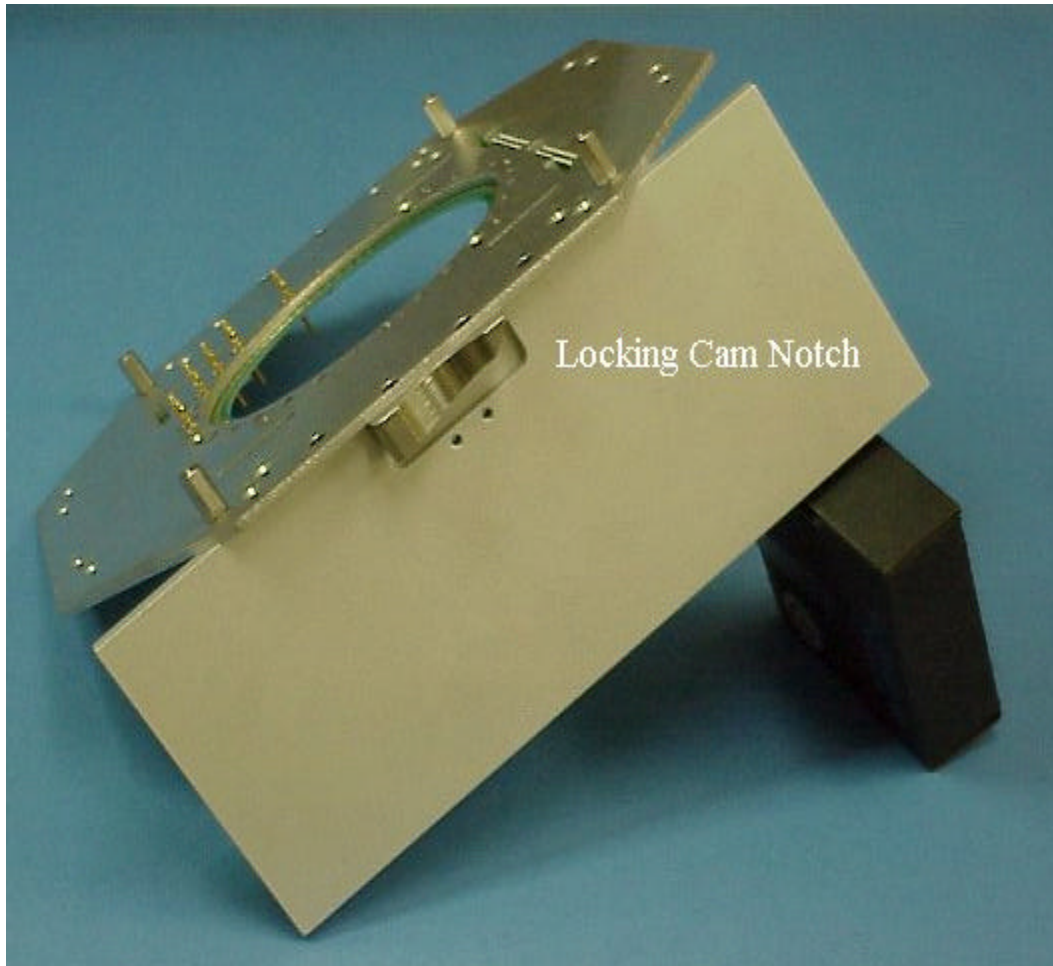


Figure 1
Fixture Side Installation

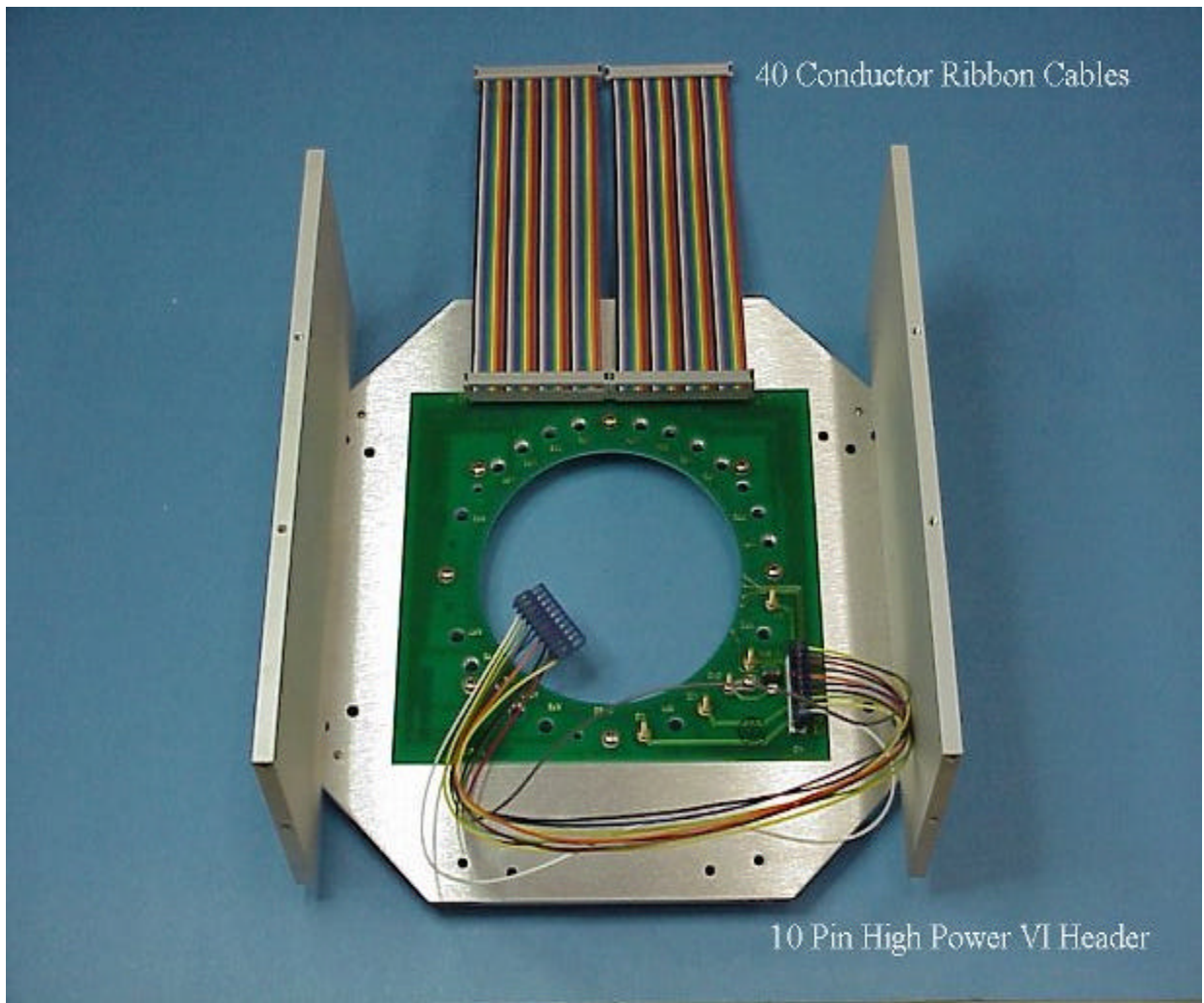


Figure 2
Fixture Side Installation

B) Top Plate Assembly:

1. Install the required **pogo pins** for the application using the **alignment tool** provided in the RiK0013A or RiK0014A kit (Fig 3). The pogo pin inserts need to be pressed into the pogo housings prior to this step.
2. After pogo pin installation, attach the **carrier board** to the **Aluminum top plate**, RiK0012A, with the lettering visible (See Figure 4).
3. Install **SMA to MCX adaptors** were needed, as determined by the fixture schematic for the application. These should not be torqued greater than **15 inch pounds** . See Figure 5.
4. As determined by the application's fixture schematic, jumper the designated tester resources to the specific pogo pins on the carrier. See Figure 5. Make sure the VI RTNS and VRTNS are connected to ground. Also make sure that GREF is attached to GND.

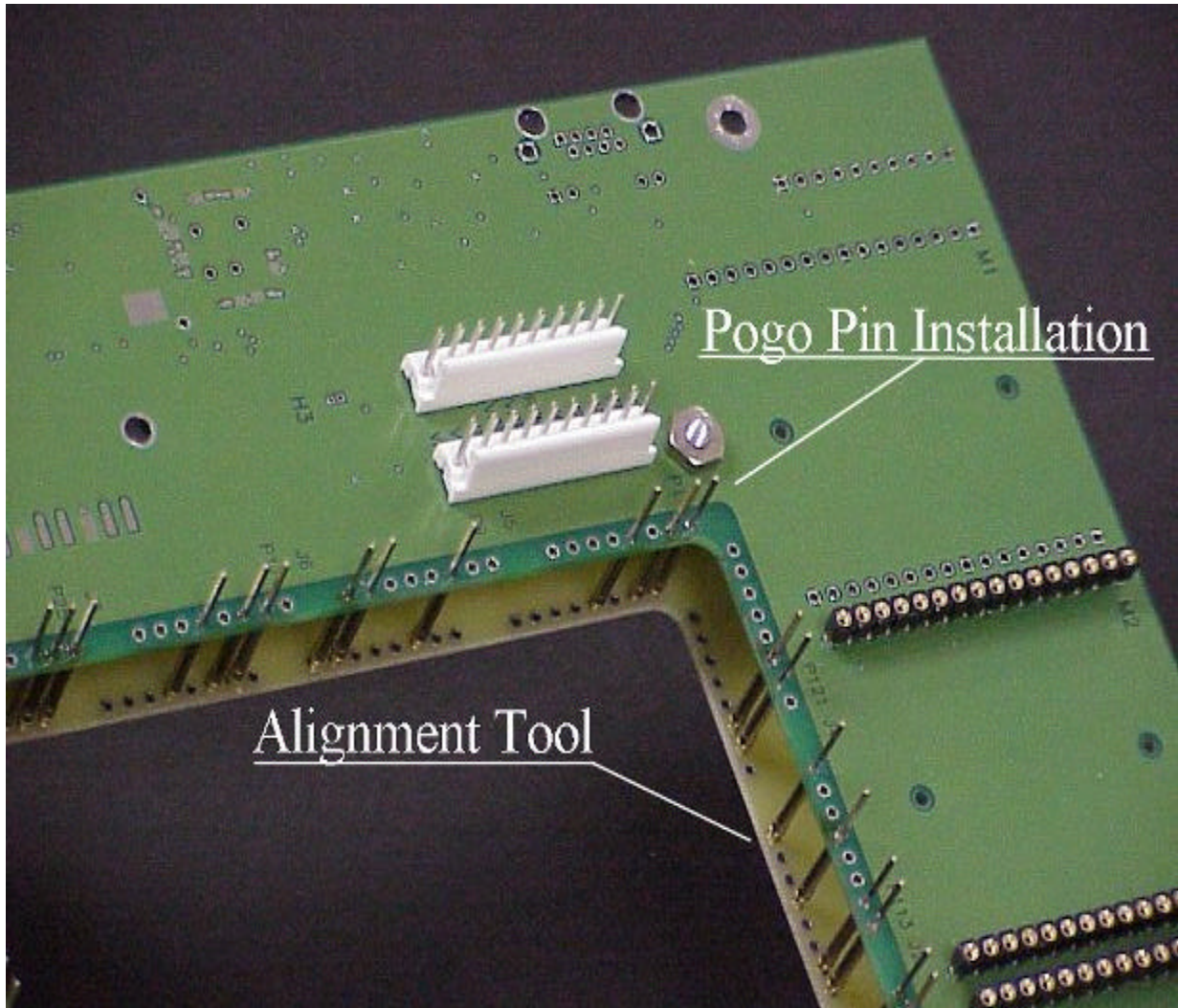


Figure 3
Pogo Pin Installation

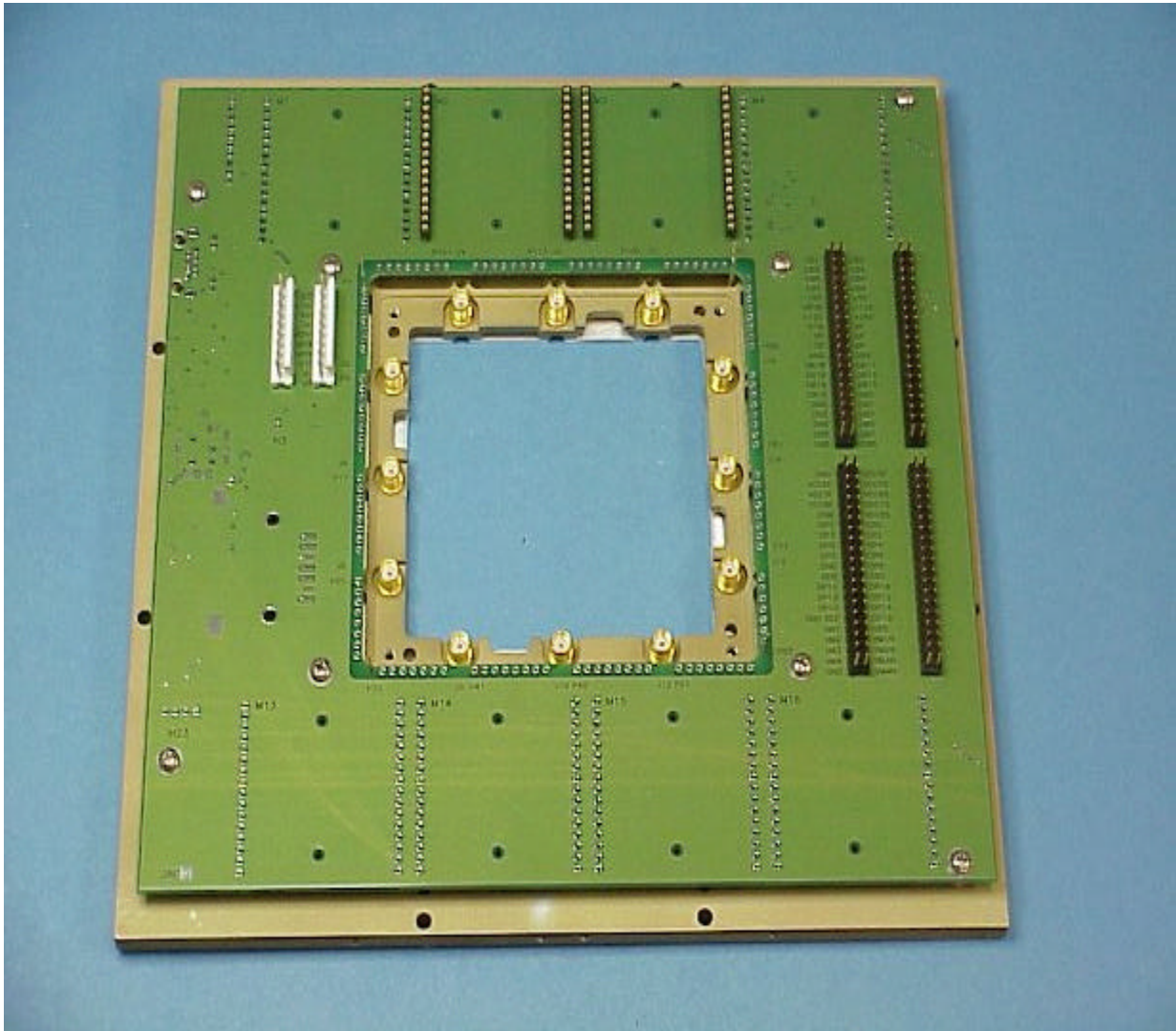


Figure 4
Carrier Installation

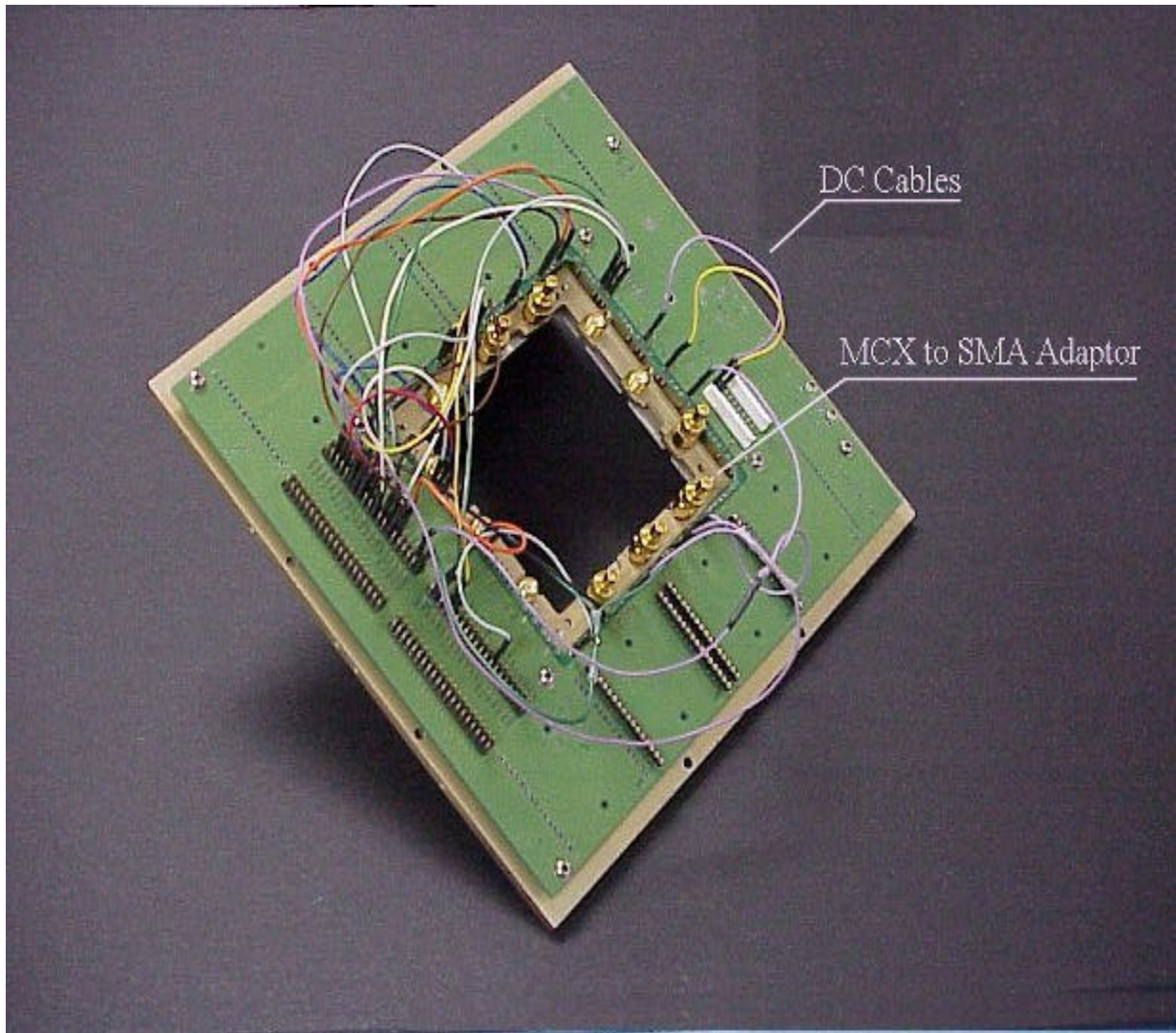


Figure 5
RF Adaptors and DC Harness Installation

C) RF Cable Installation:

1. Choose the required **RF cables** for the application. For most applications this will be a **SSIS to MCX** (RiK0001A) coaxial cable. Specialty cable assemblies are available from ROOS but are not listed in the **Standard Fixture Kits List** shown above. On the bottom plate assembly, place the cabled end into the **RF** port assigned according to the fixture schematic. See **Figure 6** for washer orientation. Attach the other side of the connector by threading it back on from the opposite side of the fixture plate. Tighten the connection using two 7/32 open end wrenches. Be careful not to over torque the connection (**Figure 7**). Suggested torque is not to exceed 15 inch pounds.
2. The **Waveform Cables** (RiK0002A) are installed by pushing in the **DINF** connector from the top side of the **Bottom Plate Assembly** into the required **WF** port location (**Figure 8**).

Warning: Once the RF (SSIS to MCX) cables are installed allow them to launch from the pogo circuit board for 1 inch before bending. Bending them at the SSIS connector directly can result in connector damage both on the fixture and on the test head.

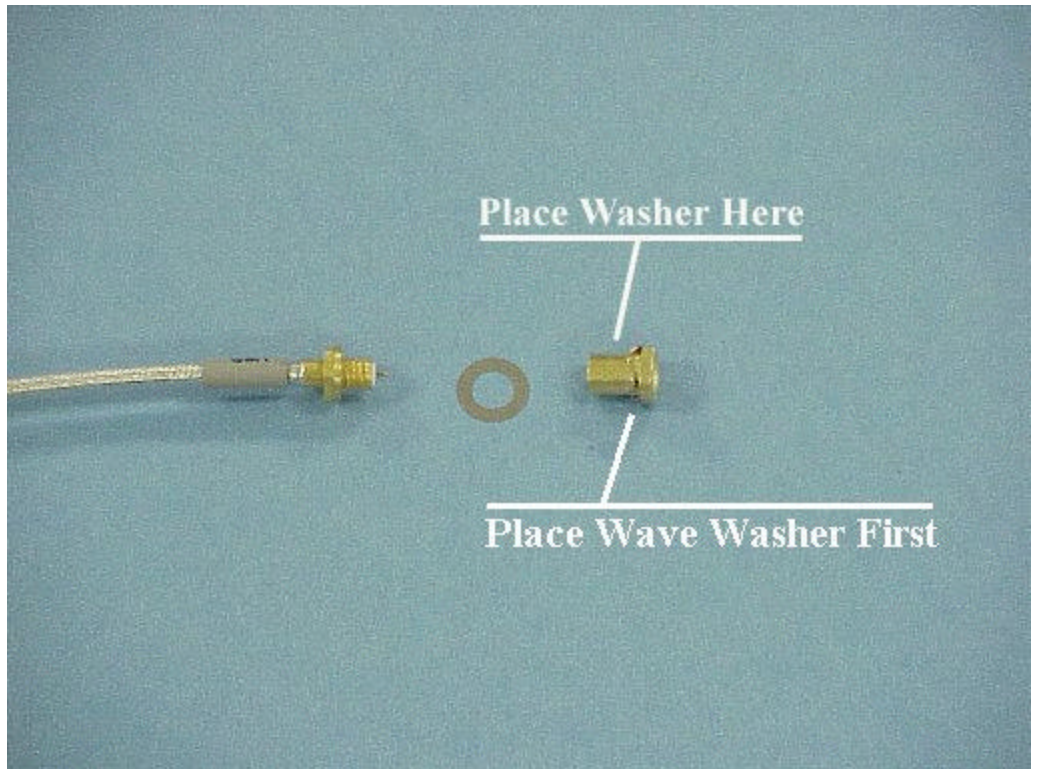


Figure 6
Washer Orientation

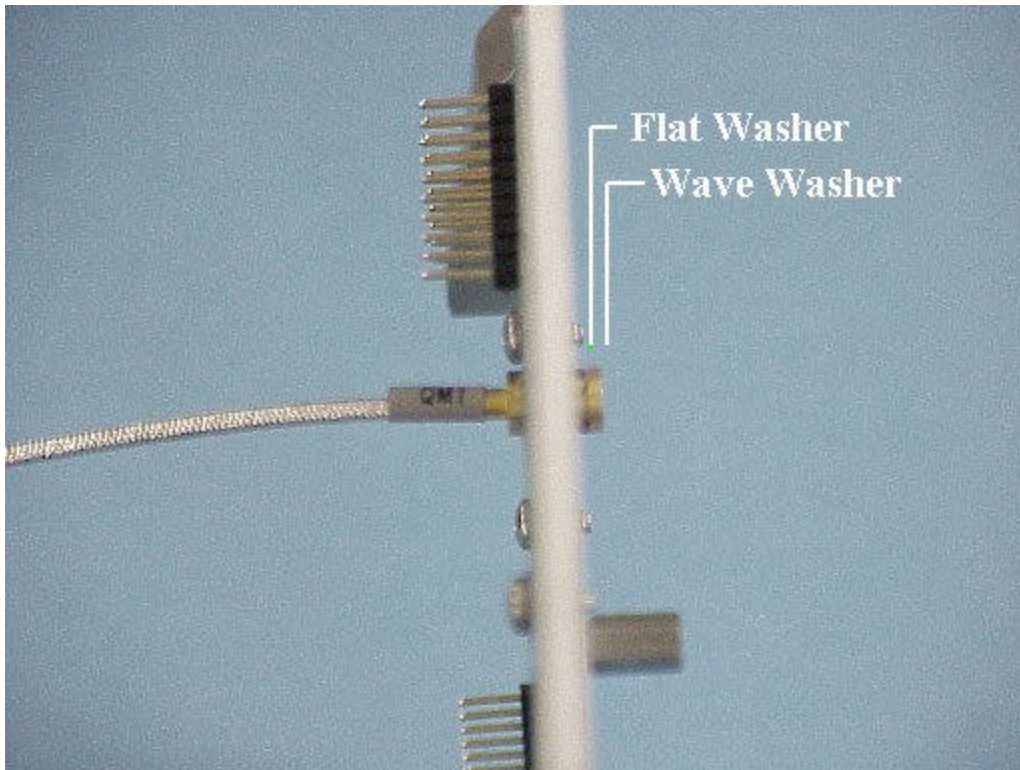


Figure 7
RF Cable Installation

Warning: Once the RF (SSIS to MCX) cables are installed allow them to launch from the pogo circuit board for 1 inch before bending. Bending them at the SSIS connector directly can result in connector damage both on the fixture and on the test head.

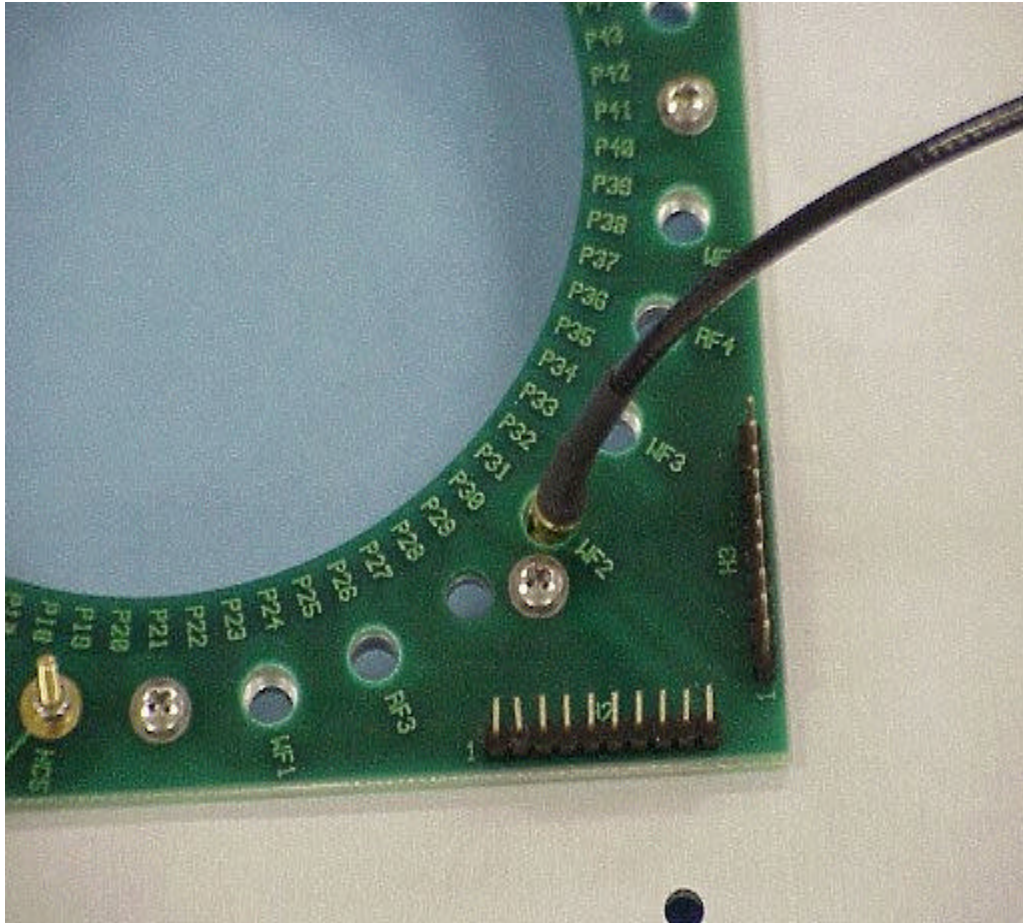


Figure 8
WF Cable Installation

D) Finishing the Assembly:

1. Attach the **top plate assembly** to the **bottom plate assembly** as shown in [Figure 9](#). This is not the final configuration but will assist access during the debug process.
2. Attach the **RF cables** and the **WF cables** to their designated RF connections on the top plate. These locations are determined by the fixture schematic for the specific application. See [Figure 9](#). Also attach the **Power VI** harness and the **40 conductor ribbon cables**.

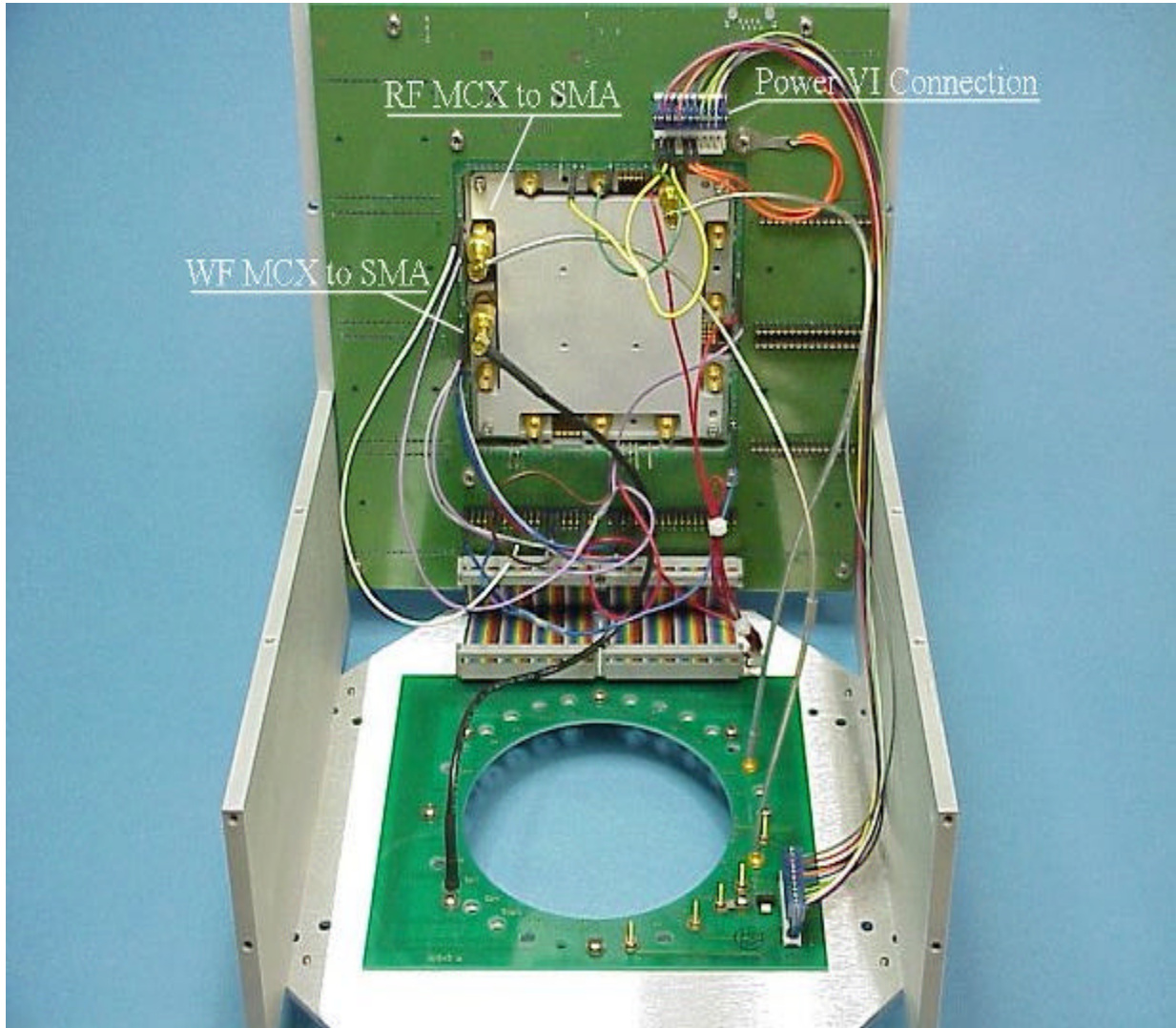


Figure 9
Finished Fixture Assembly

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What does the Software Fixture do?

The software fixture provides to the tester the schematic representation of the hardware fixture. This is important for several reasons.

- It provides the proper RF path definitions to which calibration data can be passed and saved.
- The path definitions also provide proper switch settings for any RF switches that may exist in the fixture.
- The type of calibration required for each DUT Pin Interface is also defined by the Software Fixture.
- Proper standard calibration routines for each fixture created are also defined.

Major Steps:

1. Create the [Software Fixture](#).
2. Choose the [Fixture Calibration Routines](#).

Creating a Software Fixture:

1. From the **Admin Window** select **Test** then **Fixtures** and then **NEW** within the fixtures window.
2. A fixture type will be requested with several choices being provided ([Fig. 1](#)). After choosing the fixture type, you will be asked to name the new fixture.
3. Activate the newly created fixture found in the **Fixture** window. Make sure that the intended fixture is highlighted in red ([Fig. 2](#)).
4. Serialize the fixture by using a RBMC over the fixture icon and then selecting "Get Serial Number" from the pull down menu. It will be recorded and saved automatically.
5. Using a right hand mouse button selection, choose the **Edit** choice from the menu. A **Fixture Definition** window will open ([Fig. 3](#)).
6. By selecting **ADD** on the right side of the **Fixture Definition** window a **Path Definition** window will open ([Fig. 4](#)). It is here that you will define the path of each pin between the **DUT** and the **Test Head**.
7. Begin the path definition for each pin by selecting the **DUT Interface Pin** field. To view the default choices for this field, click on the arrows next to this field using a left mouse button click.
8. Once the **DUT Interface Pin** has been defined, select the **Test Head Pin** field and choose the desired **Test Head** connection from the default list. Also choose the **Calibration Type** required for this path.
9. An optional description of the path may be typed into the description field by simply selecting this field and typing the description desired.
10. The **Mode** field is usually used to define different paths that have common **DUT Interface Pins** and **Test Head Pins**. For example one path may have an attenuator between DutRF1 and RF2. The other path may be a through path between DutRF1 and RF2. "**Attenuator**" could be typed into the mode field for the one path and "**Thru**" could be typed into the other.
11. The **Switch** field is used to define the state of Cbits used to control fixture related devices. In the example of step 10 it would be used to control a pair of SPDT switches. There are a total of eight Cbits associated with the passive carrier. If Cbit control is needed a series of eight Xs, 1s, or 0s would be typed into this field. The Cbit designation in this string would go be CBit 8 to Cbit 1 from left to right XXXXXXXX1 means that CBit 1 is held high. X = Don't Care, 0 = Low, and 1 = High.
12. Select **OK** after each path definition. Note that the **Path** field will be updated in the **Fixture definition** window ([Fig. 5](#)).
13. After defining all of the fixture pins select **OK** in the **Fixture Definition Window**.

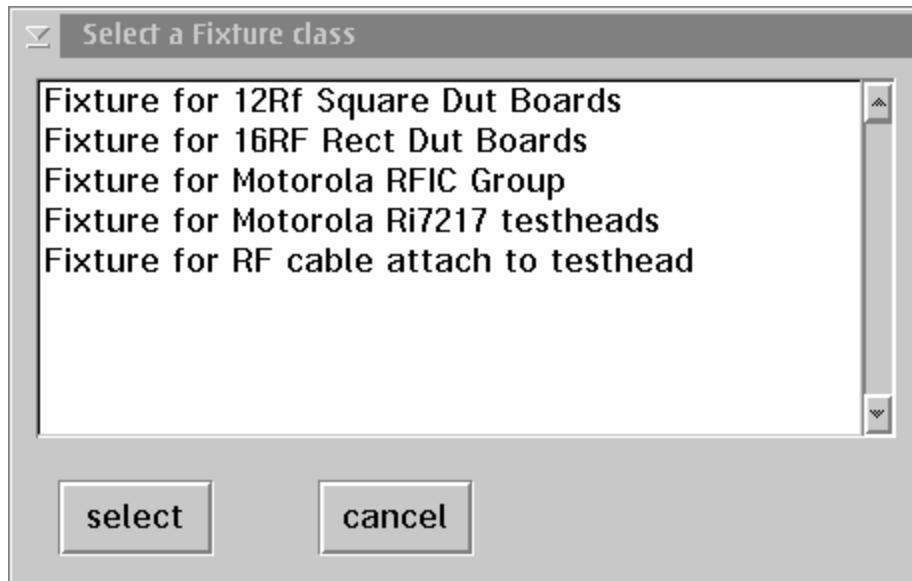


Figure 1
Fixture Class

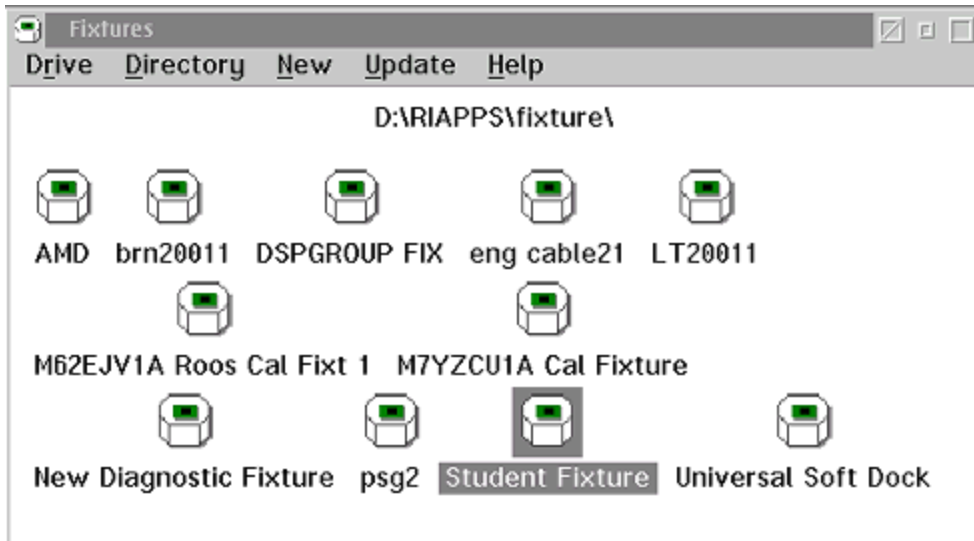


Figure 2
Fixture Icon

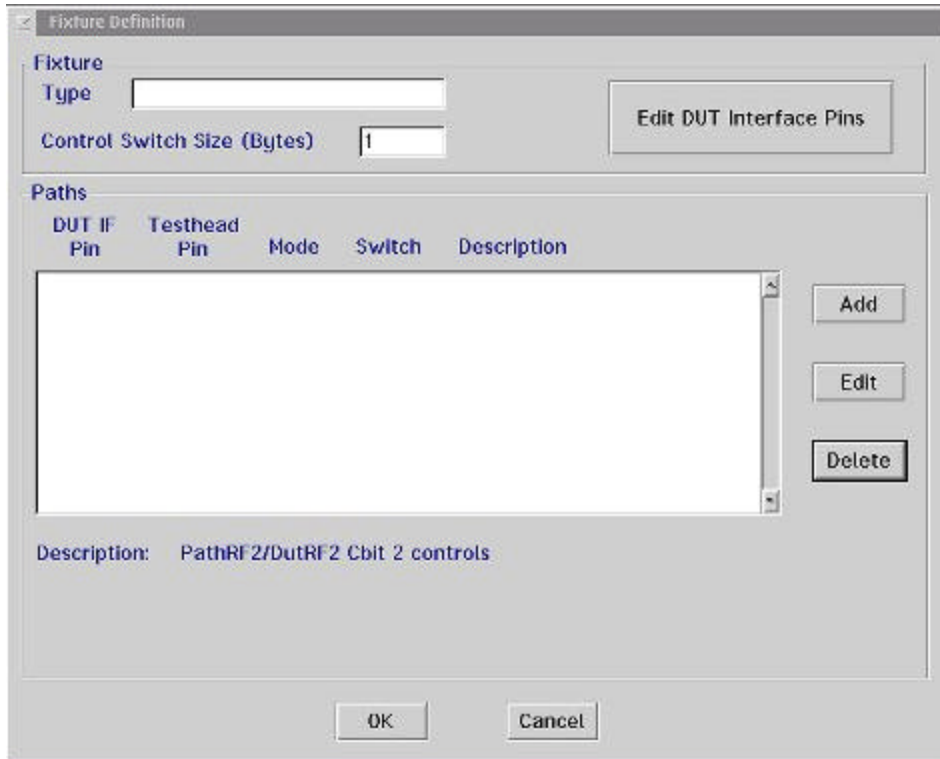


Figure 3
Fixture Definition Blank

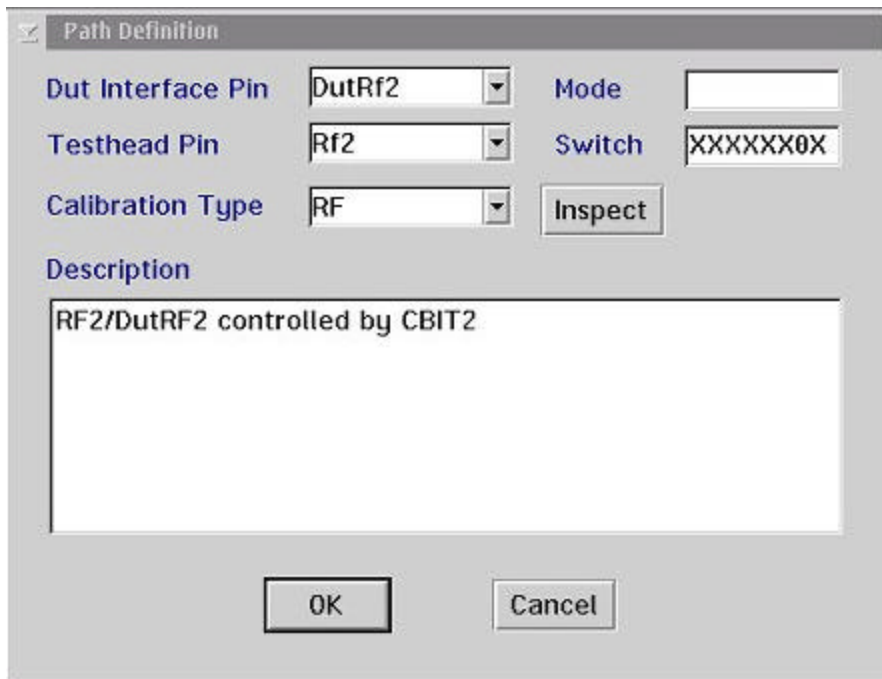


Figure 4
Path Definition

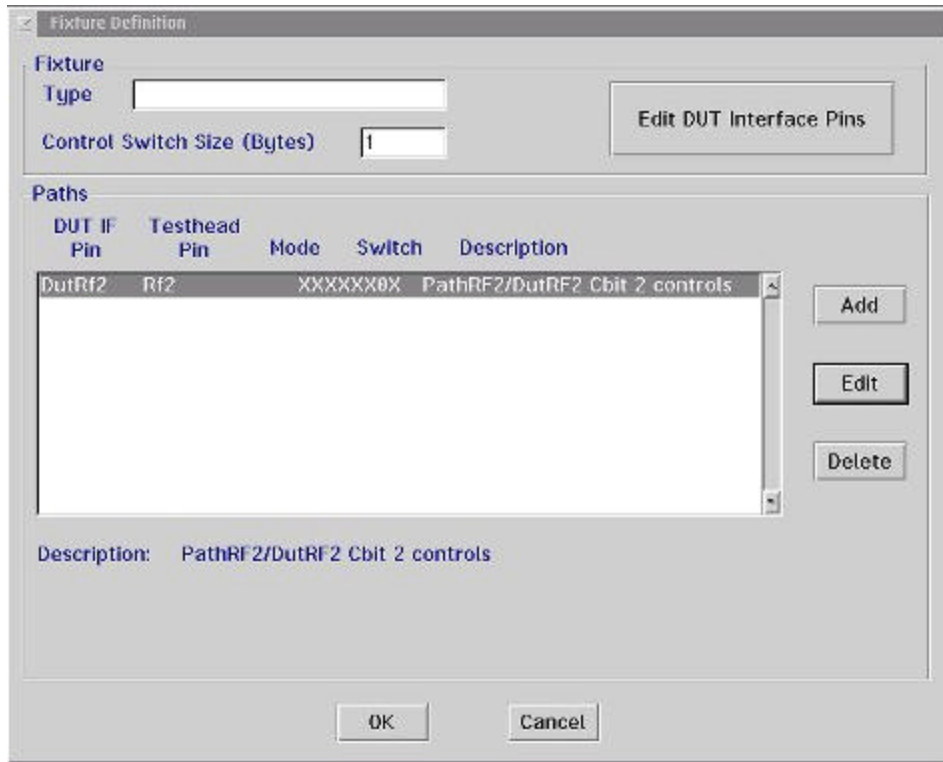


Figure 5
Completed Path Definition

Choosing Calibration Routines:

1. Make sure that the desired fixture is activated and highlighted. While the fixture is highlighted (Fig. 2) use the right mouse button to display a fixture menu. Choose **Calibrate** within the menu. A **Select Fixture** window will open with a list of fixture calibration types (Fig. 6). Choose **Standard** for the test fixture type. Options for this selection will be discussed later.
2. Once you have done this a **Fixture Calibrations** window will open with the name of the specific fixture you have highlighted (Fig. 7). Choose **Programs** from the top menu bar and then **ADD**. A list of available calibration routines will appear in list form (Fig. 8). Select the Standard calibration test plan which corresponds correctly to the path you are trying to calibrate. The selected calibration test plans will automatically be added to the **Fixture Calibrations** window.
3. Answer **YES** when asked if you want to save the settings.



Figure 6
Calibration Routines

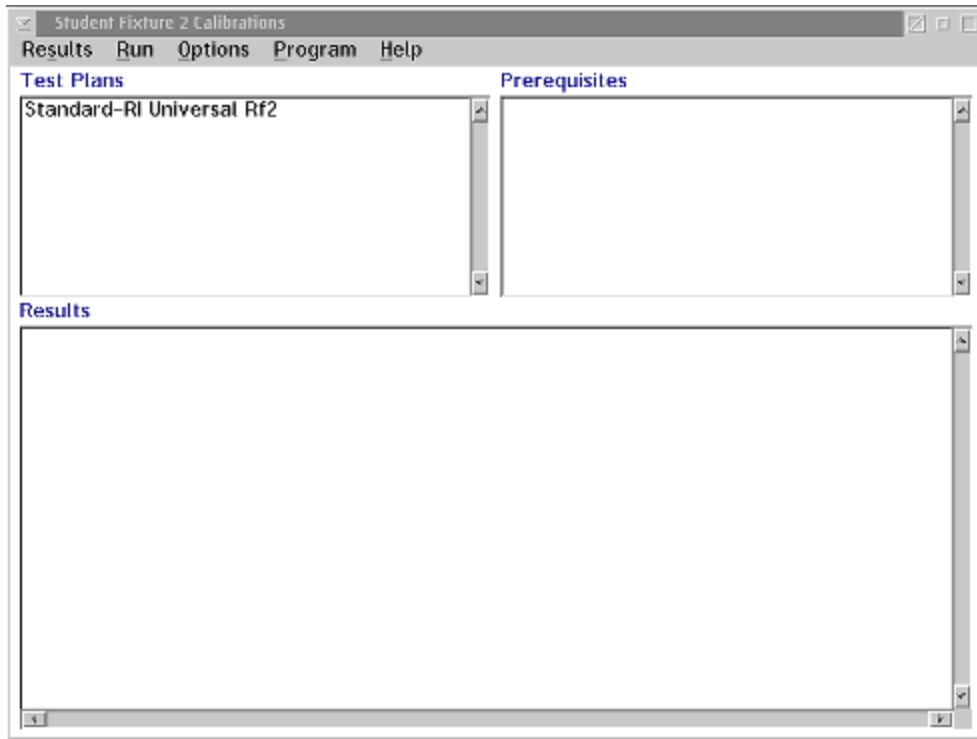


Figure 7
Fixture Calibration Window

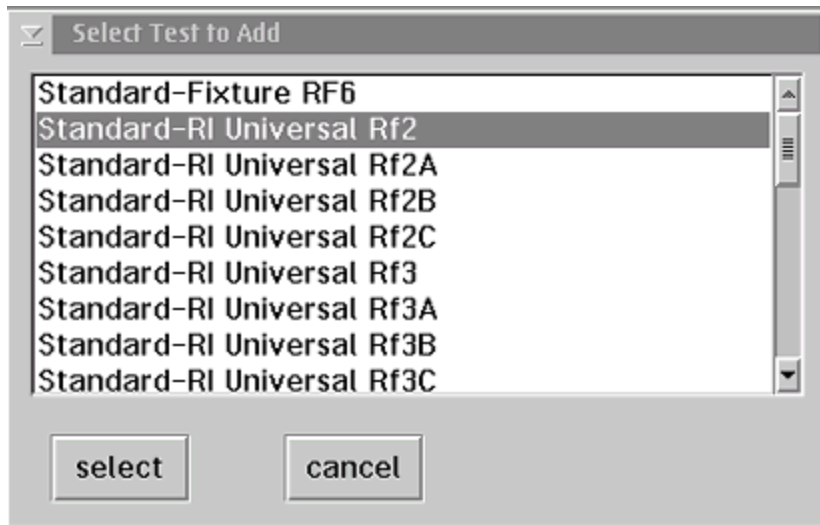


Figure 8
Adding Tests



Document Purpose:

To give the test engineer a step oriented approach to editing the dut interface pins during the creation and modification of a software fixture.

Steps:

1. From the **Admin Window** select **Test** then **Fixtures**. The **Fixtures** window as shown in [Figure 1](#) will then appear.
2. Highlight the specific fixture that is to be edited.
3. Using the right mouse button activate the pull down menu for that fixture and select **Edit**. A **Fixture Definition** window will appear as shown in [Figure 2](#).
4. Additional paths can be added by selecting **Add** at the right hand side of the window and using the **Paths Definition** window that will appear ([Fig. 3](#)).
5. If a **new DUT Interface Pin** needs to be added to the DUT Interface Pin List then select the **Edit DUT Interface Pins** button at the top upper right. A **DUT Interface Pins** window will appear ([Fig. 4](#)). Editing of existing DUT Interface Pin names can also be done here. It should be noted that this capability is only allowed on fixtures of type "**Fixture for RF cable attach to testhead**".

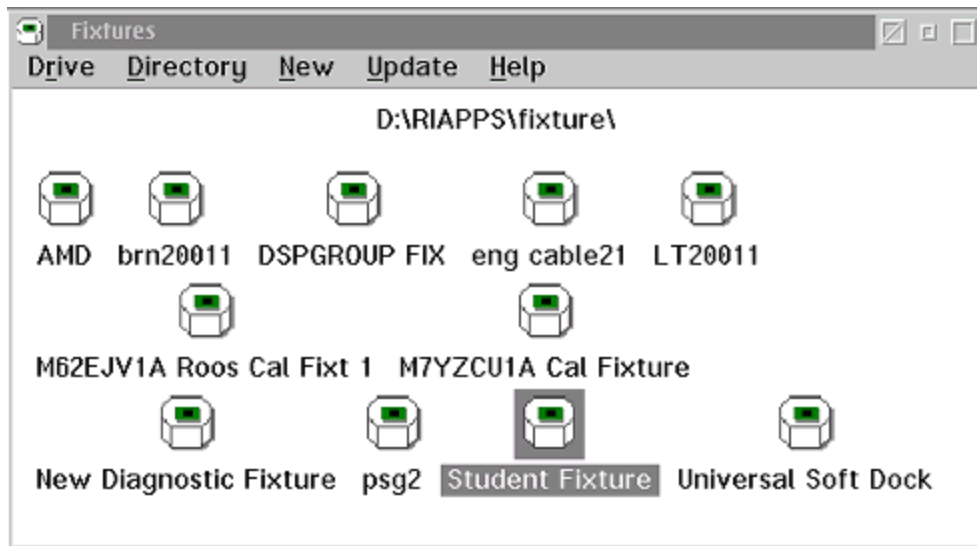


Figure 1
Fixtures Window

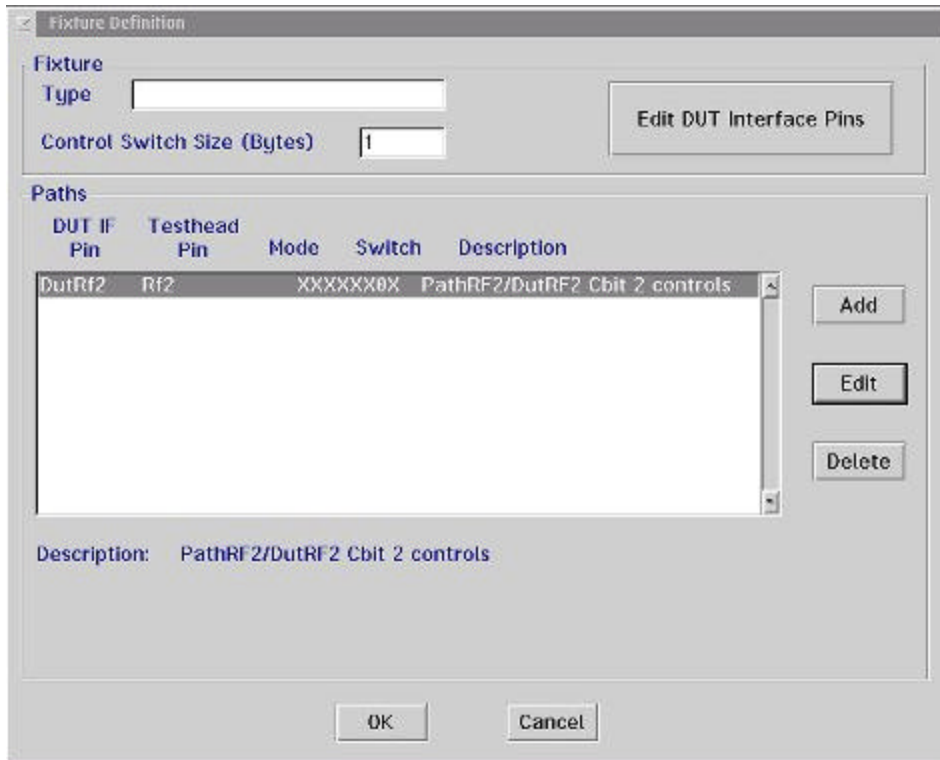


Figure 2
Fixture Definition Window

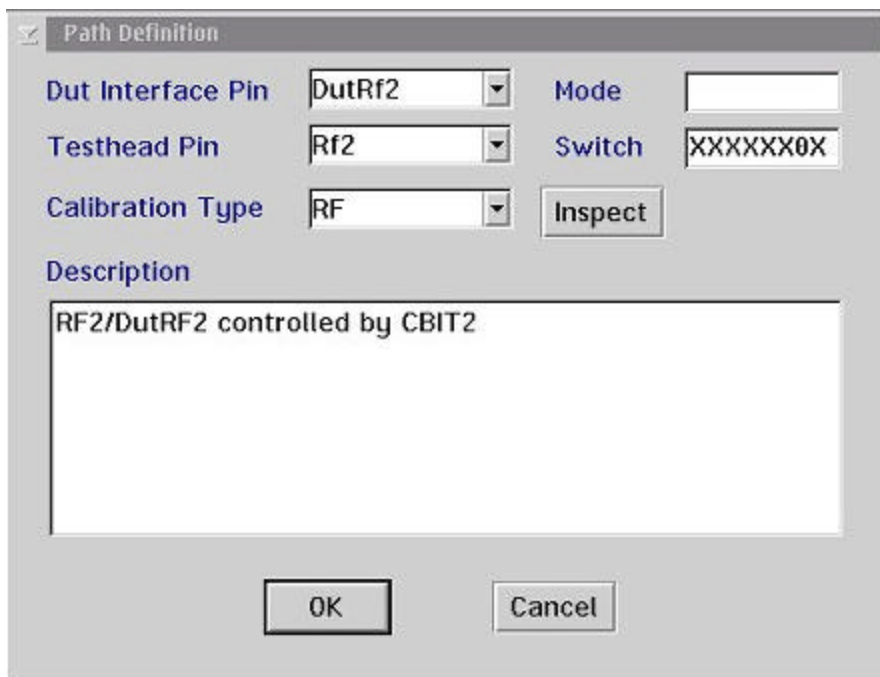


Figure 3
Path Definition Window

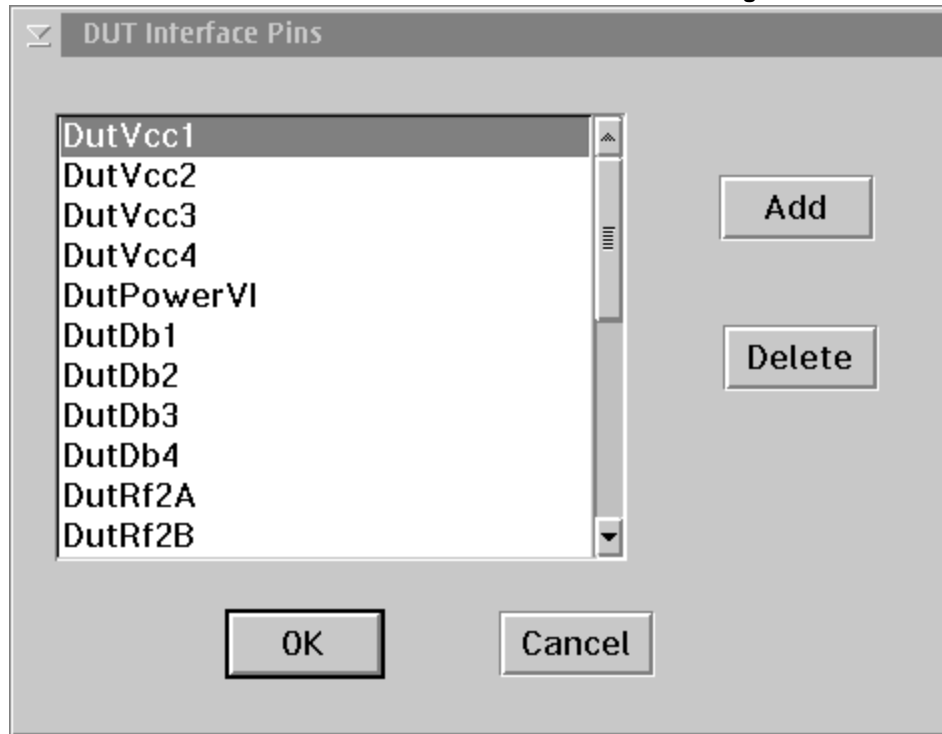


Figure 4
DUT Interface Pin Addition

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Document Purpose:

To provide the test engineer a guide in **Defining the Software DIB (DUT Interface Board)**.


What does the Software DIB do?

The Software DIB provides to the Tester a definition of the hardware DIB. This allows for the application of calibration data related to the DIB to be applied during test.

Major steps:

- Create the Software DIB.
- Edit the connections of the Software DIB.

Creating the Software DIB:

1. It is encouraged that a **Software DUT** be created before proceeding. 
2. Under the **Programmers Message Window** select **T**est and then **D**evice **I**nterfaces. At this point a **Device Interfaces** window will open up ([Figure 1](#)). Select **N**ew and a **Fixture class** window will open up ([Figure 2](#)).
3. After selecting the **Fixture class** the user will automatically be asked for the name of the new DIB.
4. After naming the new DIB the user will then be asked to select the DUT associated with the DIB as shown in [Figure 3](#). The Device Interface window will automatically be updated with the new DIB at this point.

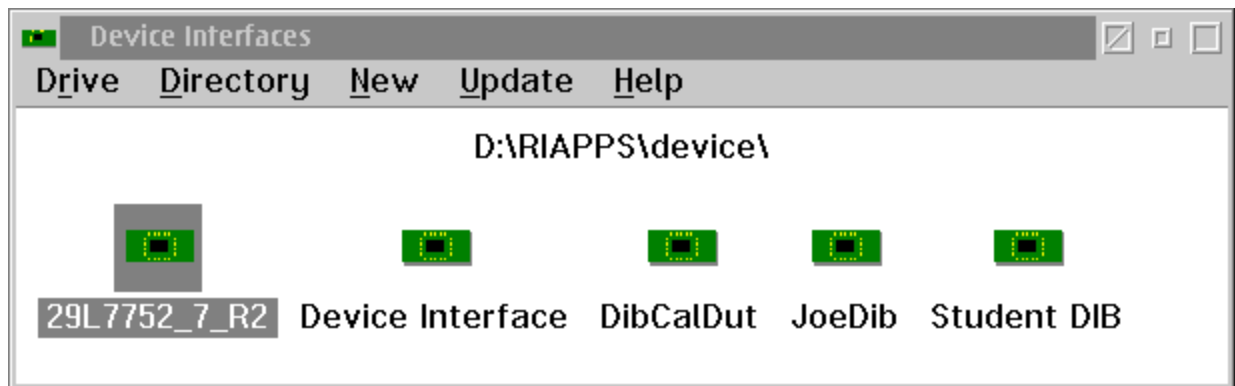


Figure 1
Device Interfaces

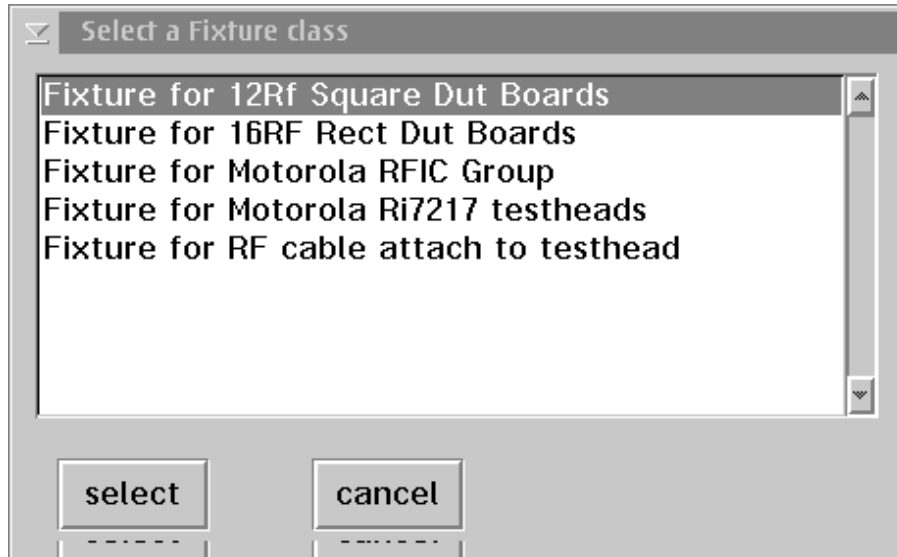


Figure 2
Fixture Class

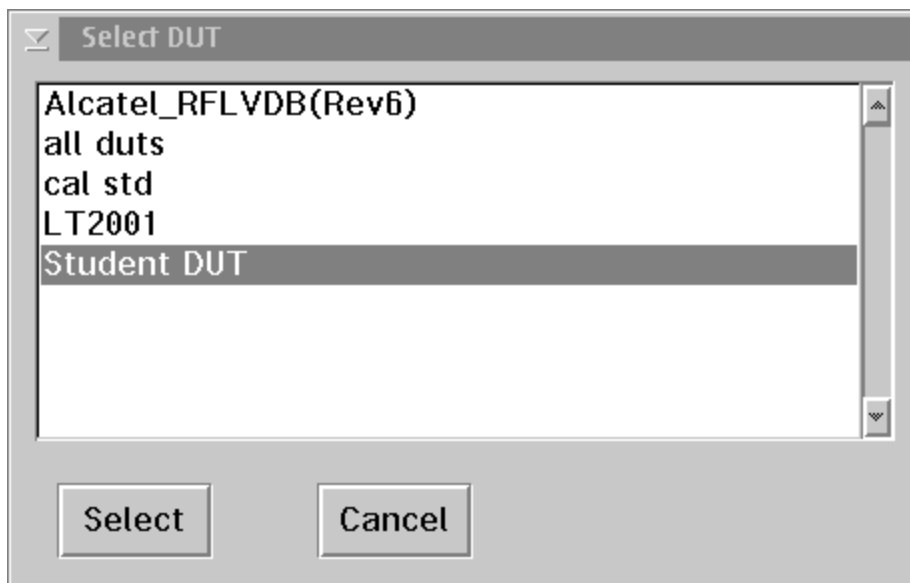


Figure 3
Select DUT

Editing the Pins of the Software DIB:

1. Highlight the **DIB** that you wish to edit as shown in [Figure 4](#). Using a right mouse button click a menu will appear. From this menu choose **Edit**.
2. A **Device Interface Definition** window as found in [Figure 5](#) will appear. It would also be helpful to have the **Pins** editing window open for the DUT intended for the DIB ([Fig. 6](#)). This is done by:
 - Selecting **Test** then **Devi**ces from under the **Message Window**.
 - Highlighting the desired **DUT** to be used and, with a right mouse button click, choosing **Pins** from the menu.
3. Make sure that the proper Fixture Name appears in the upper right hand field of the **Device Interface Definition** window. If it does not, choose from the selections provided. Also remember to choose the **Fixture Type**.
4. Enter the DIB **Type** in the upper left hand field.
5. Edit the **Fixture Connection >> Device Pin** interface by highlighting the desired path to be changed. Once you have highlighted the path choose the **Device Pin** field and select the DUT pin associated with that path. Also make sure that you select a **Calibration Type** for each pin were required. Once the **Fixture Connections** have all been defined, as shown in [Figure 7](#), select **OK** and the edit window will close.

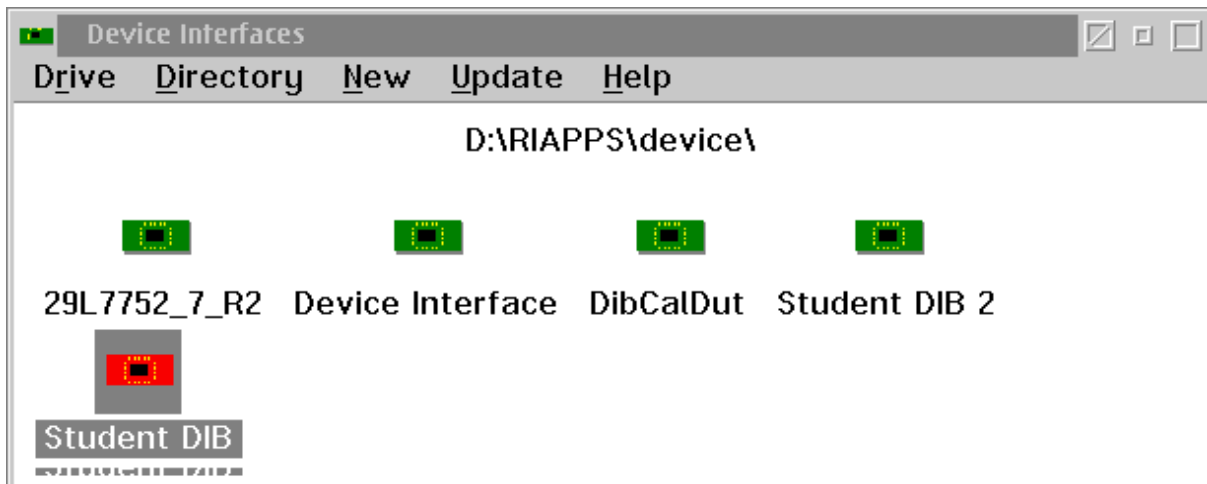


Figure 4
Device Interfaces

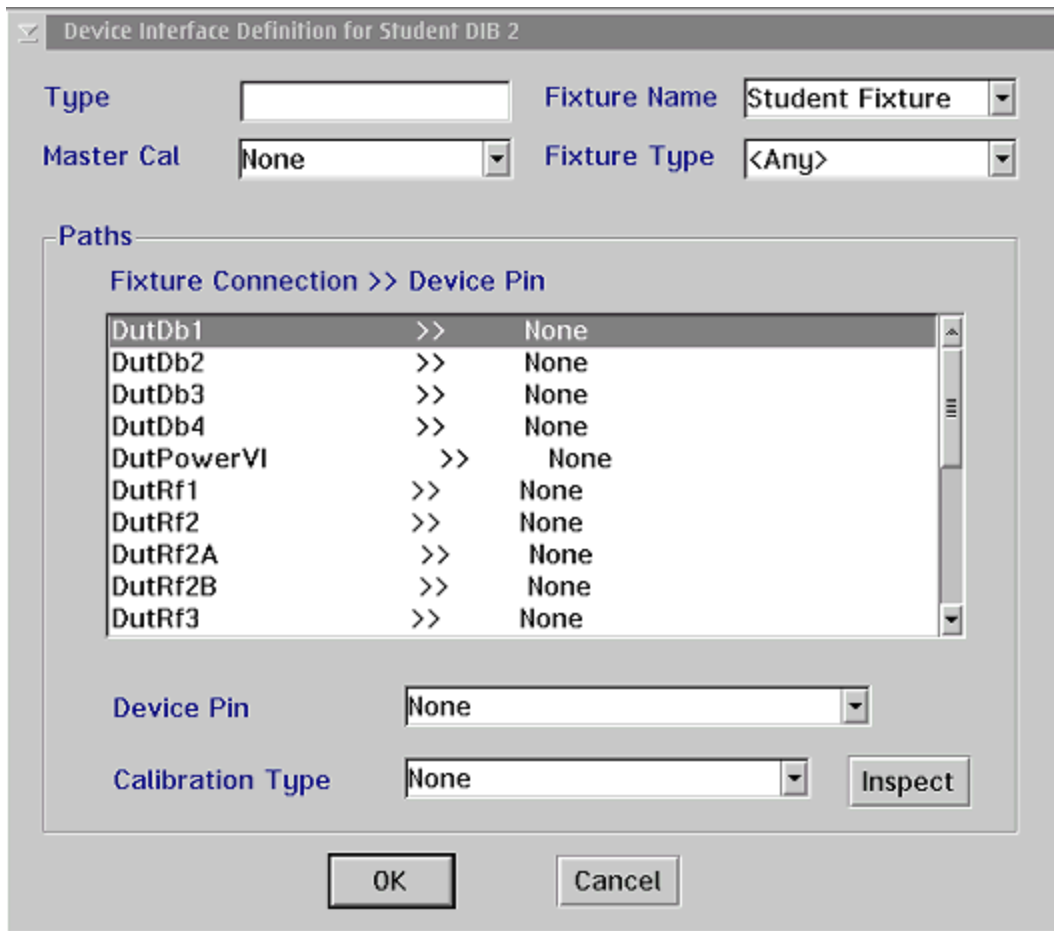


Figure 5
Device Interface Define

Pins

Number of pins:

#	Type	Description
1	RFin	LNA IN
2	Gnd	
3	DCin	S1
4	DCin	S2
5	DCin	ENBL
6	RFout	IF OUT+
7	RFout	IF OUT-
8	RFin	LO IN
9	RFin	RF IN+
10	RFin	RF IN-

Type:

Description:

Figure 6
Pin Definition

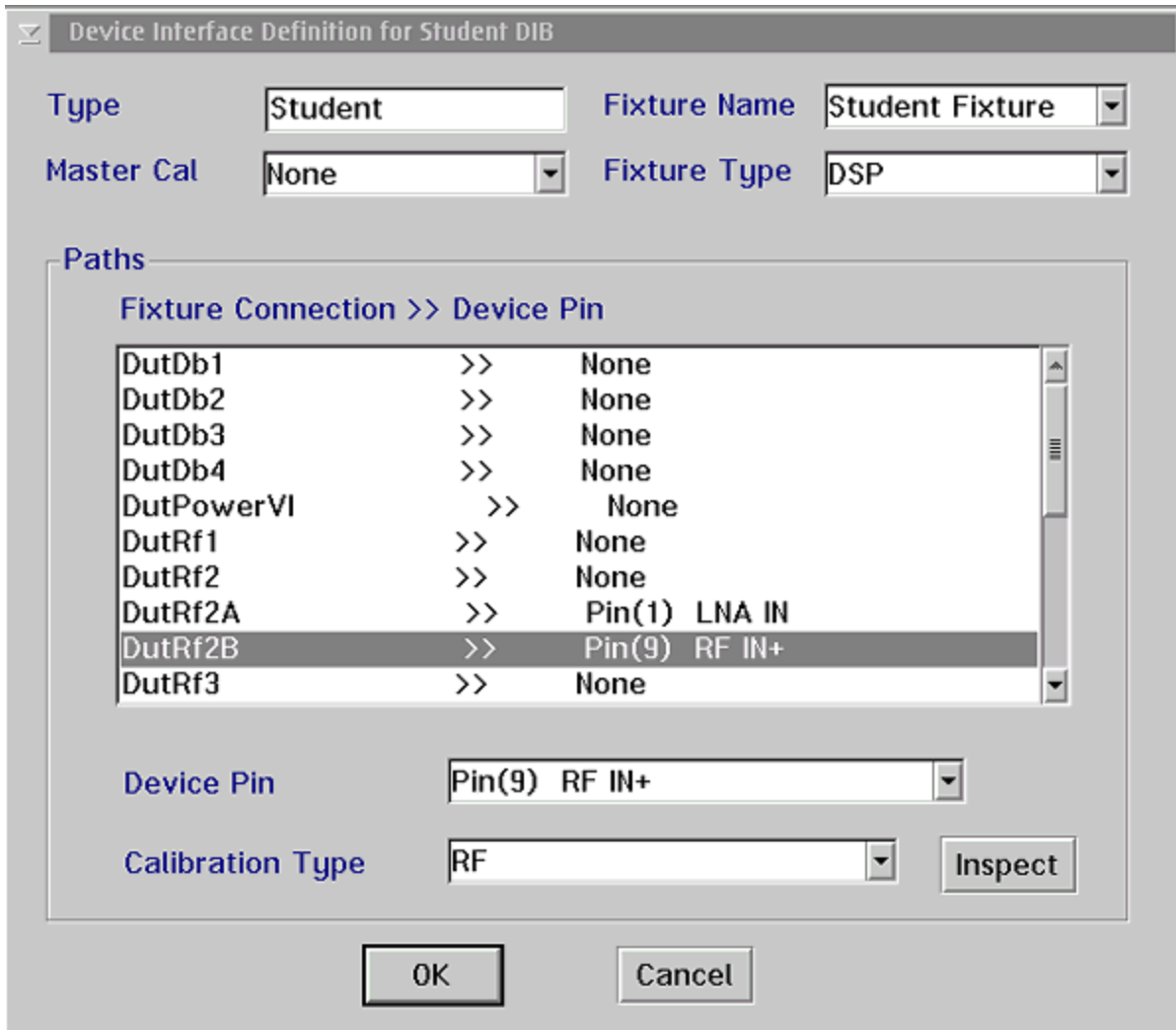


Figure 7
Defined Fixture Connections



Document Purpose:

To provide the test engineer a guide in **Creating a Software DUT** to be used with the RI 7100A tester and its associated fixturing.

What does the Software DUT do?

The Software DUT is the first step in defining how the device relates to the testers resources. Although not required, its use is encouraged in aiding the process of Software DIB and Software Fixture creation. It also provides a mapping between the device pins and the Device Interface Board.

Process Steps :

1. From the programmers **Message Window** select **Test** then **Devcies** then **New** ([Figure 1](#)).
2. After selecting **New** and **DUT** a window will pop up asking you to name the new **DUT** ([Figure 2](#)).
3. After naming the new DUT highlight it with a left hand mouse button click. Use a right hand mouse button to use the pull down menu to edit the DUT.
4. Choosing **Pins** will open an edit window for the new DUT ([Figure 3](#)).
5. Enter the number of pins for the DUT in the **Number of pins** field. After entering the number of pins repeat steps 3 and 4 to begin editing the DUT pins.
6. Highlight Pin #1 and define its type by selecting one of the options in the **Type** field. As a further option the pin can be described in the **Description** field.
7. Once you have defined all the **pin#s** and their **Types** select **OK**. [Figure 4](#) and [Figure 5](#) represent the DUT definition for the **Student DUT** as seen in [Figure 1](#).

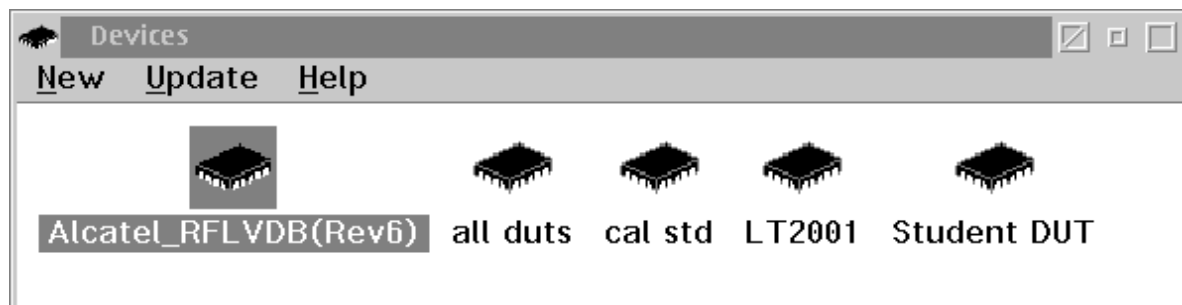


Figure 1
New Device

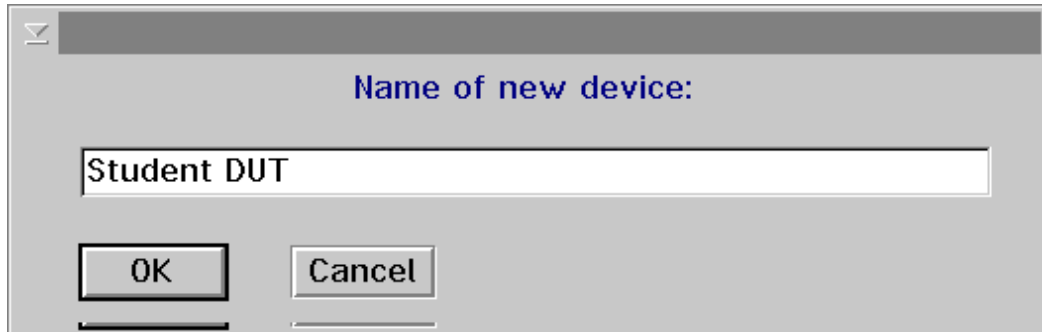
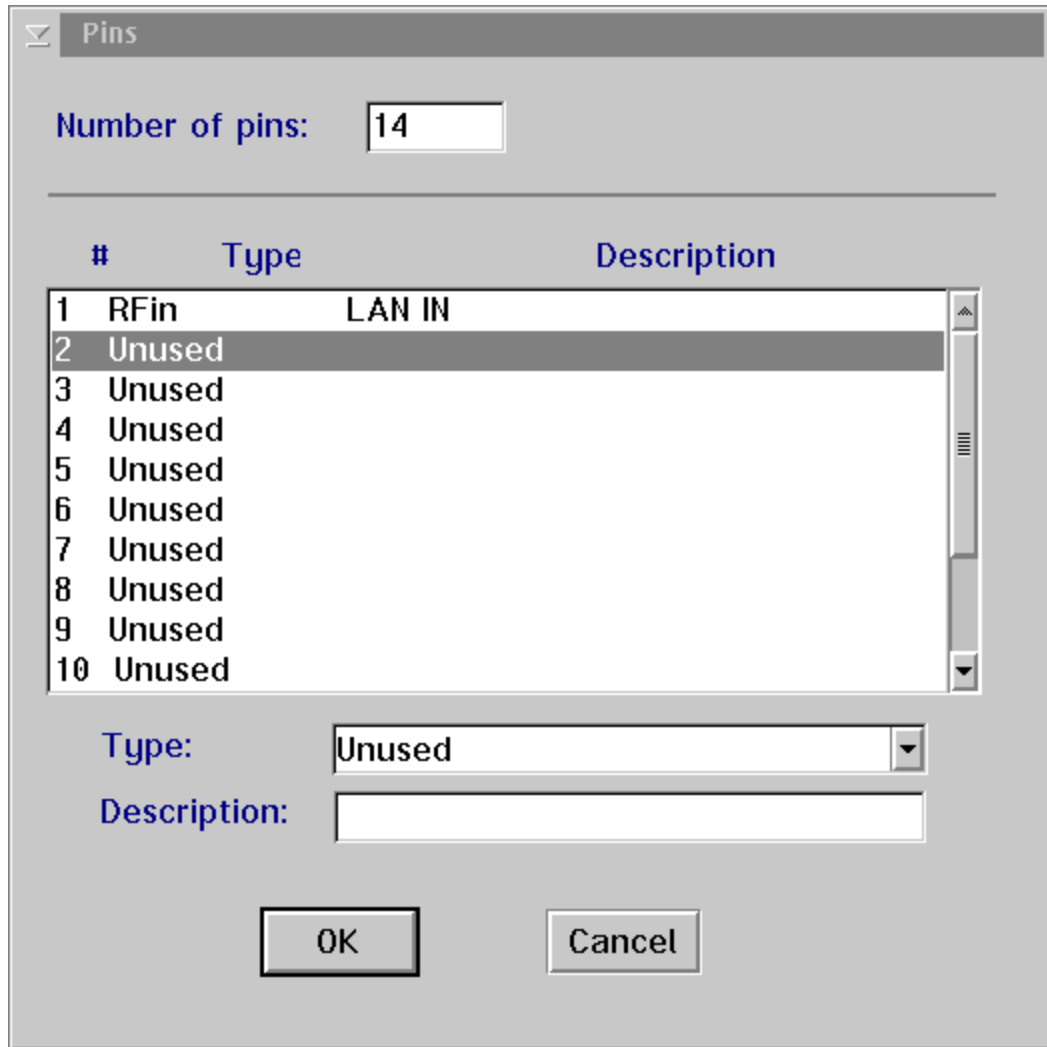


Figure 2
New Device Name



Pin Edit

Figure 3

Pins

Number of pins:

#	Type	Description
1	RFin	LNA IN
2	Gnd	
3	DCin	S1
4	DCin	S2
5	DCin	ENBL
6	RFout	IF OUT+
7	RFout	IF OUT-
8	RFin	LO IN
9	RFin	RF IN+
10	RFin	RF IN-

Type:

Description:

Figure 4

DUT Definition

Pins

Number of pins:

#	Type	Description
5	DCin	ENBL
6	RFout	IF OUT+
7	RFout	IF OUT-
8	RFin	LO IN
9	RFin	RF IN+
10	RFin	RF IN-
11	DCin	VCC2
12	DCin	VCC1
13	Unused	
14	RFout	LNA OUT

Type:

Description:

Figure 5

DUT Definition



Document Purpose:

To provide the test engineer a guide in **Calibrating the Hardware Test Fixture** used with the RI 7100A tester. This document will describe how to perform calibration on the RF ports of the test fixture.

Steps:

1. Install the hardware fixture to be calibrated onto the test head.
2. From the **Admin Window** select **Test** then **Instruments**. Activate the desired **Calibration Kit** and the desired **Power Meter** from the instruments available ([Fig. 1](#)).
3. From the **Admin Window** select **Test** then **Fixtures**. The **Fixture** window will open as found in [Figure 2](#).
4. Activate the **Fixture** to be calibrated.
5. Click on the fixture using the right hand mouse button. Choose **Calibrate** from the drop down menu that will appear.
6. Choose the proper Fixture Calibration Program type from the selections list ([Fig. 3](#)). Once you have done this a Calibrations window will appear with all the calibration programs selected for that fixture ([Fig. 4](#)).
7. At this point you have the option to select some or all of the programs to be run. Once you have done this select **Run** and **Selected**.

Caution: During the compile of a calibration test plan all cal data associated with the test plan will be reset in the fixture. This means that a **Cancel instead of **OK** at the operator response has already reset the fixture cal data to default values.**

8. Follow the operator prompts as they appear on the screen.

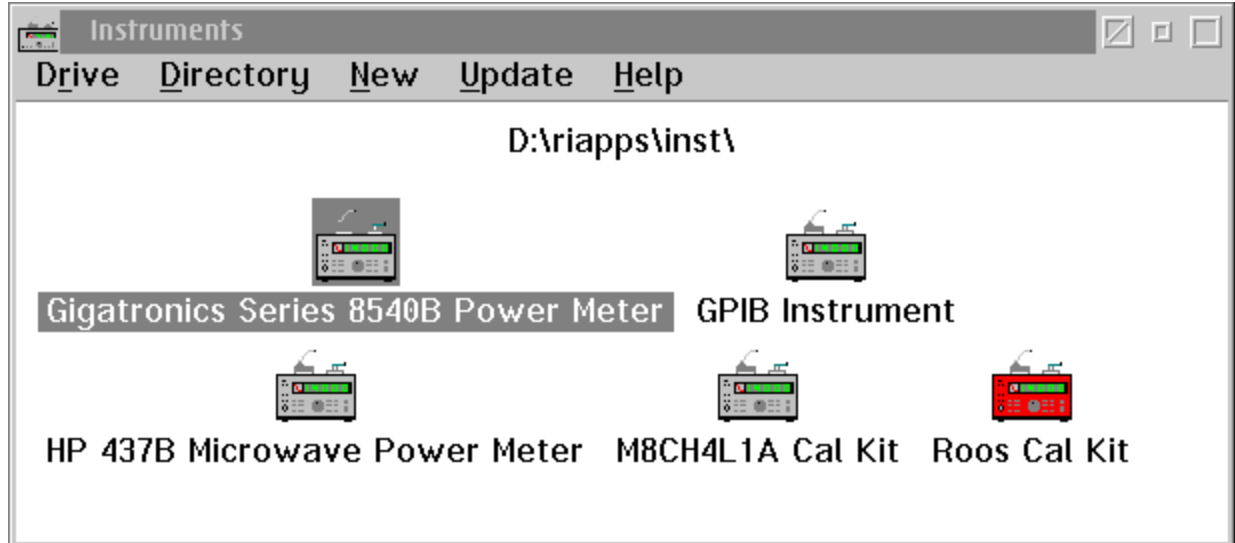


Figure 1
Instruments Available

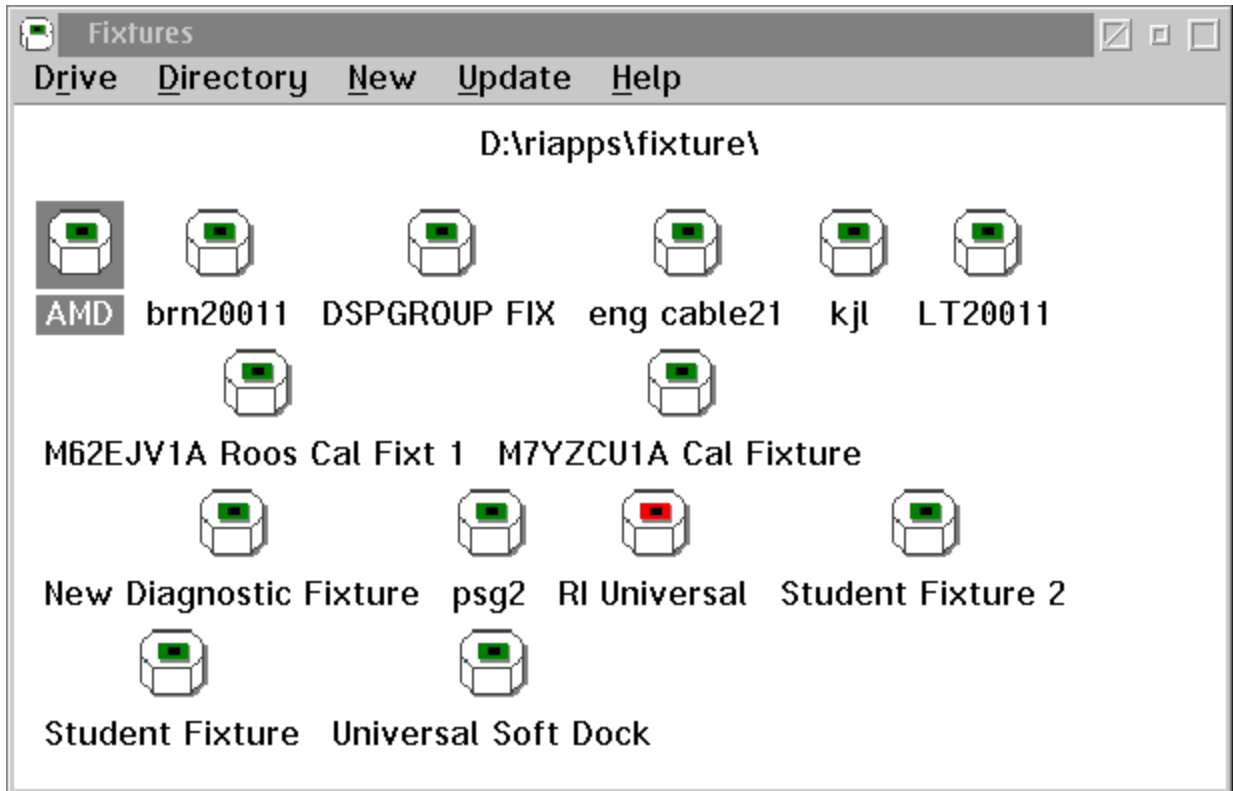


Figure 2
Fixtures

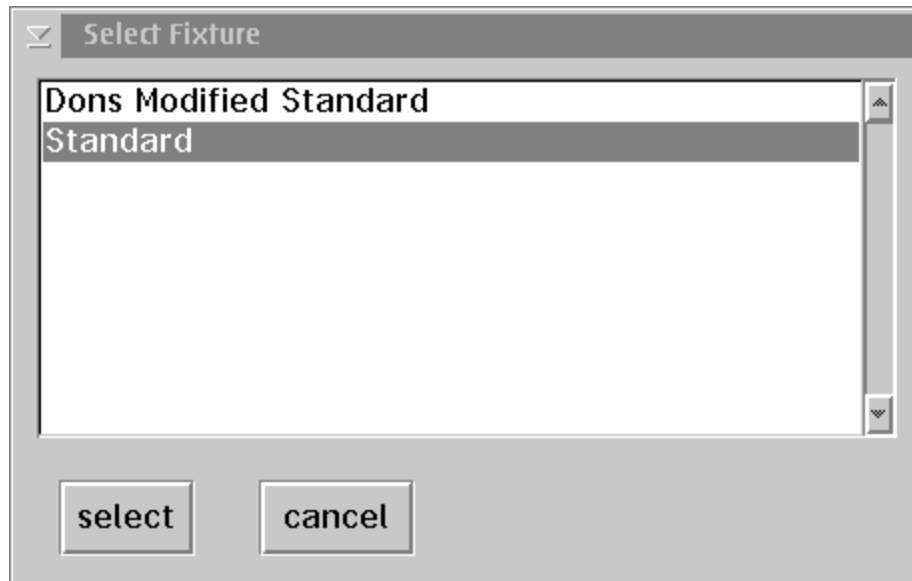


Figure 3
Calibration Test Plan Type

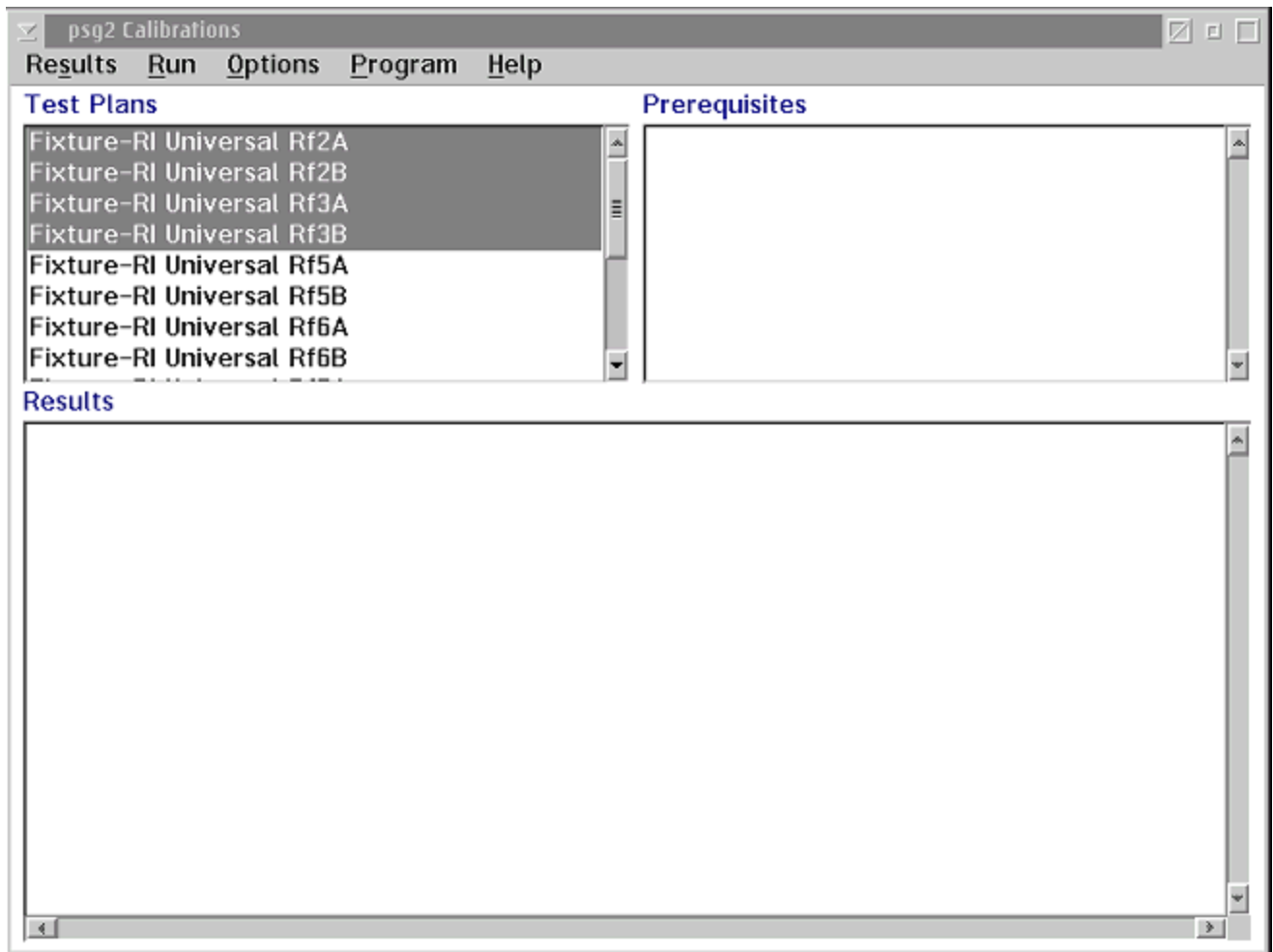


Figure 4
Calibration Test Plans

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Checking the Fixture Calibration Data (Automated)

Purpose:

To give the test engineer the ability to check the fixture calibration data.

Checking and Saving the Fixture Calibration Data:

1. Inspect calibration data before saving it to the fixture. Begin by high lighting the fixture you are calibrating. Using a right mouse button click select **Calibration Inspect** from the menu.
2. From the list of Fixture RF paths that will appear, high light the path that is to be inspected (Figure 1). Use a right mouse button click and choose **View/ Rectangular** (Figure 2)as selections. A plot of the calibration data will appear.
3. Use the graph format choices to set up the graph with proper units and references for viewing. A sample set of data is provided in Figures 3-6.
4. Once the fixture calibration data has been check it can be saved. To do this high light the activated fixture and with a right hand mouse button click bring up the selection menu. Choose **Save Calibration** to save the data just taken to the fixture.

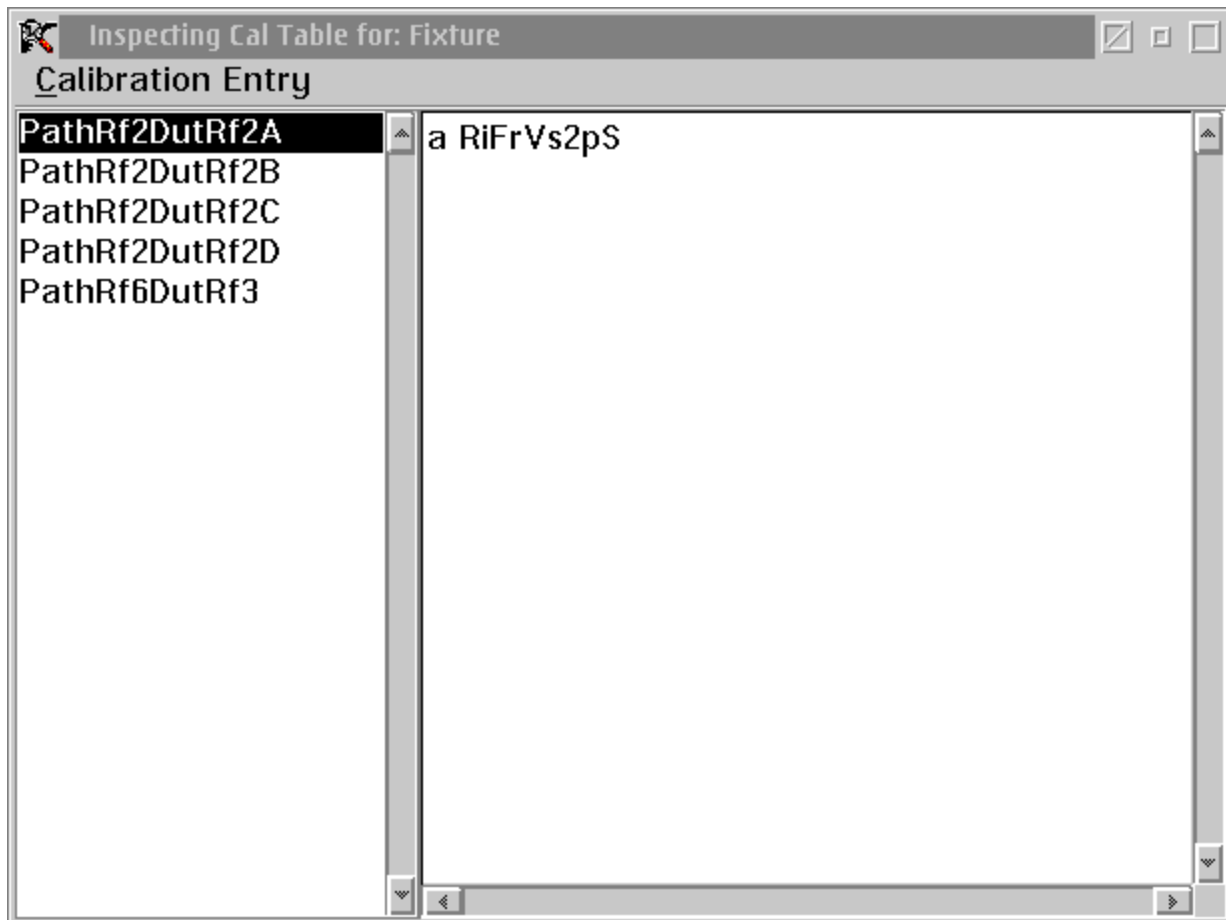


Figure 1

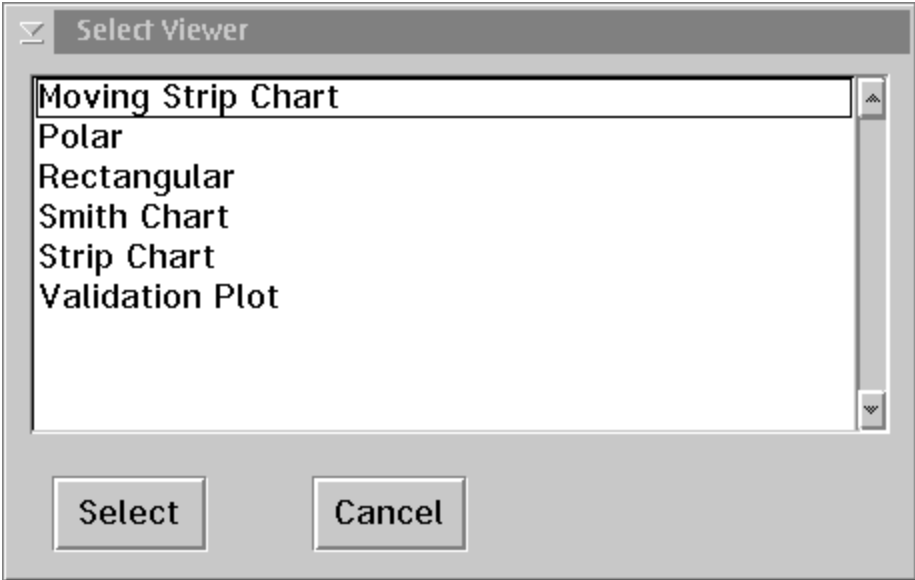


Figure 2

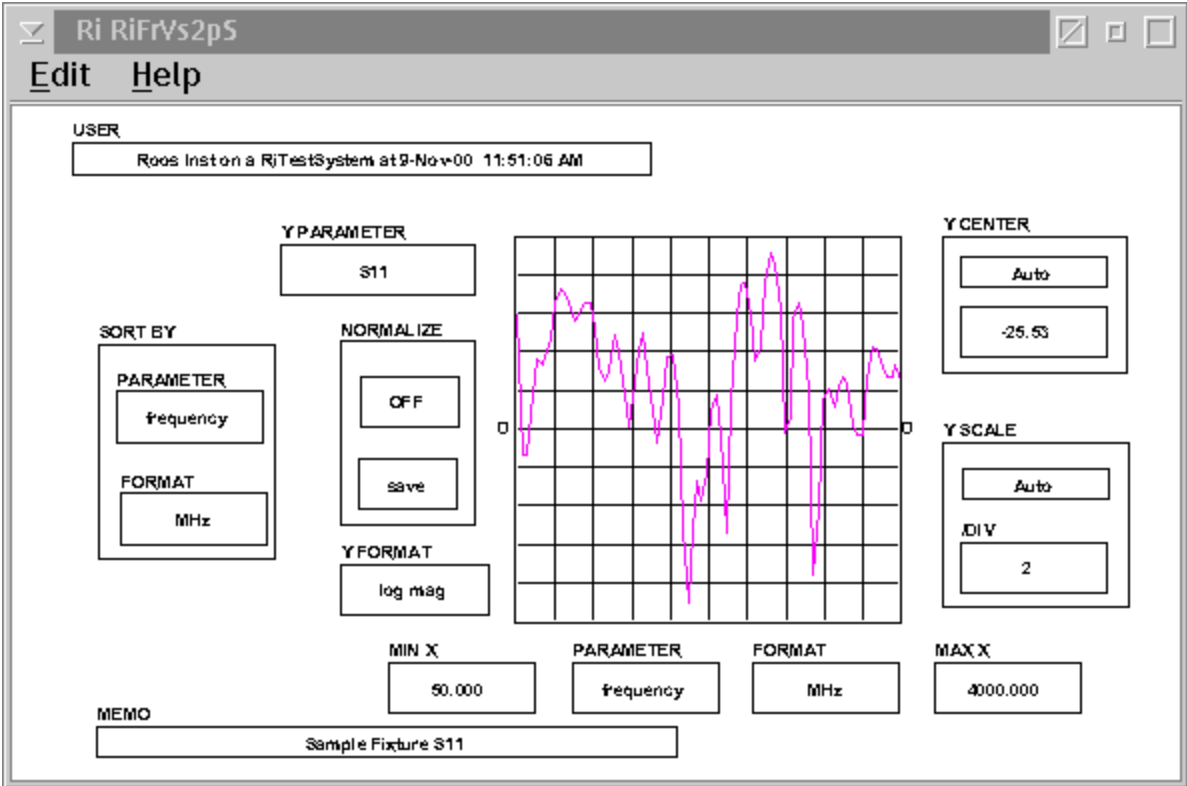


Figure 3

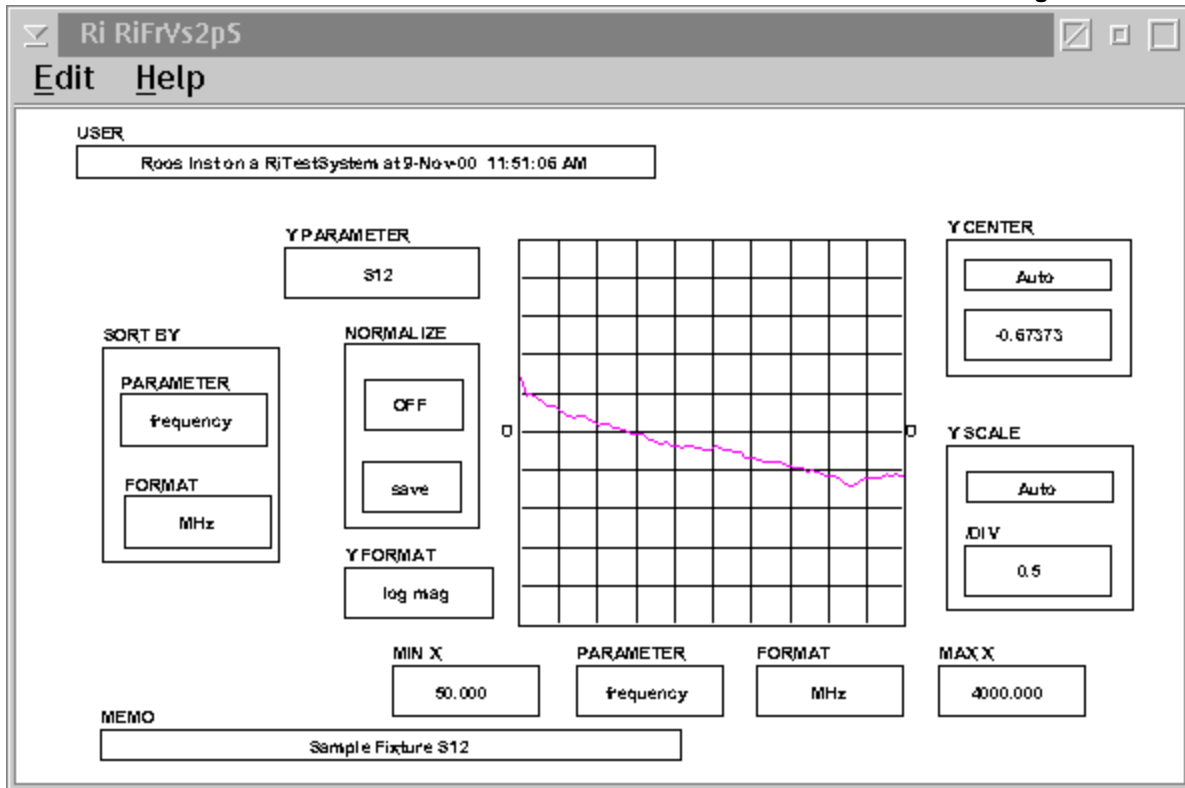


Figure 4

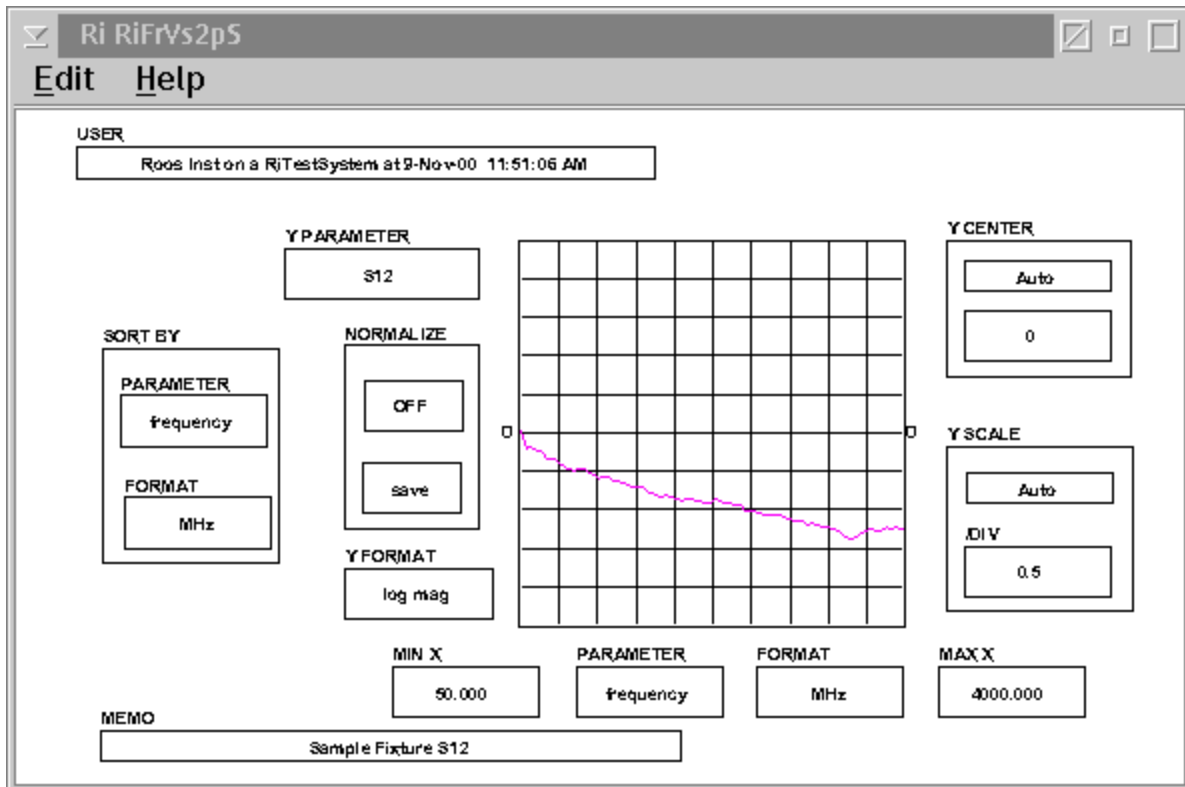


Figure 5

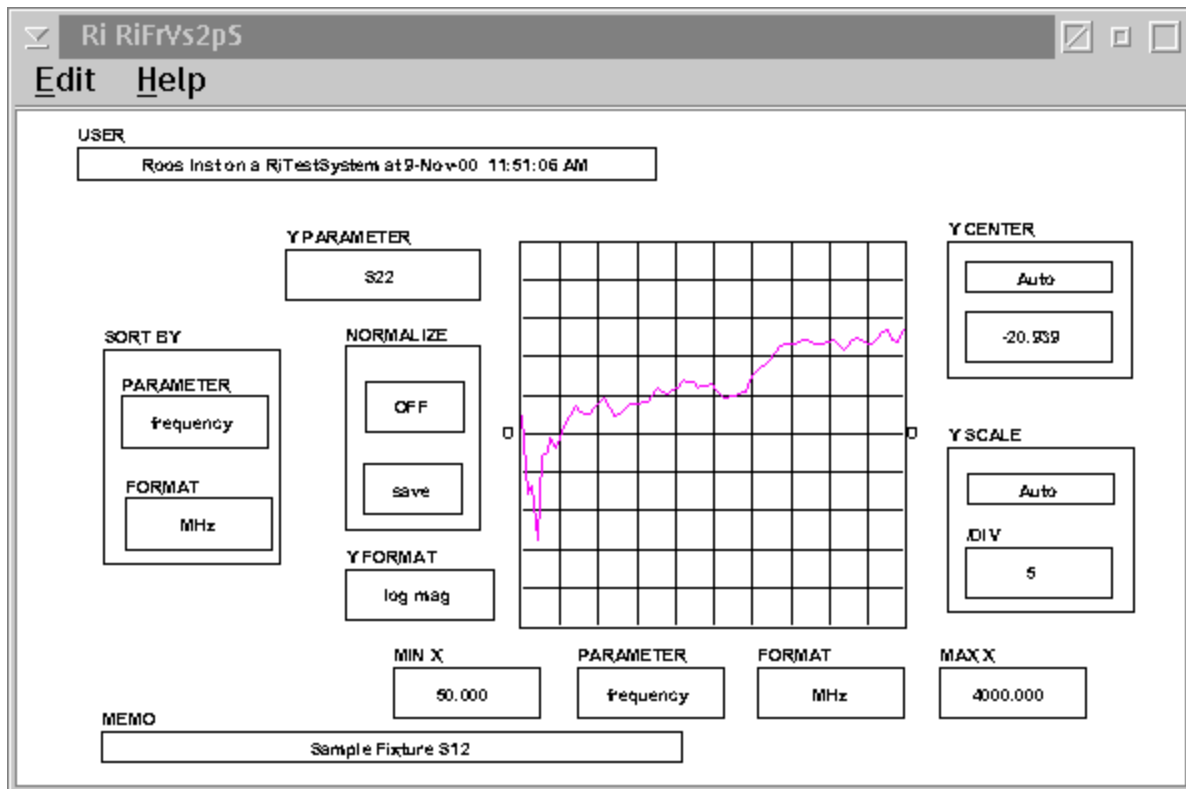


Figure 6

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Document Purpose:

To provide the test engineer a guide in **Calibrating the DIB** (DUT Interface Board) used with the RI 7100A tester. This document will describe how to perform calibration on the RF ports of the DIB.

Steps:

1. From the **Admin Window** select **Test** then **Instruments**. Activate the desired **Calibration Kit** (Fig. 1). If a calibration is to be performed on a port associated with **RF5** of the **Test Head** make sure that a **Power Meter** is also activated.
2. From the **Admin Window** select **Test** then **Fixtures**. The **Fixtures** window will open as shown in Figure 2. Activate the fixture to be used with the DIB being calibrated
3. From the **Admin Window** select **Test** then **Device Interfaces**. The **Device Interfaces** window will open as shown in Figure 3.
4. Activate the **DIB** that needs to be calibrated.
5. Using the right mouse button activate the pull down menu for the **DIB** and select **Calibrate** from this list. The **Calibration** window for the DIB will open with a selection of calibration test plans (Fig. 4).
6. Select the specific testplans that are desired and then select **Run** then **Selected** at the top of the window. Follow the operator prompts as they appear.

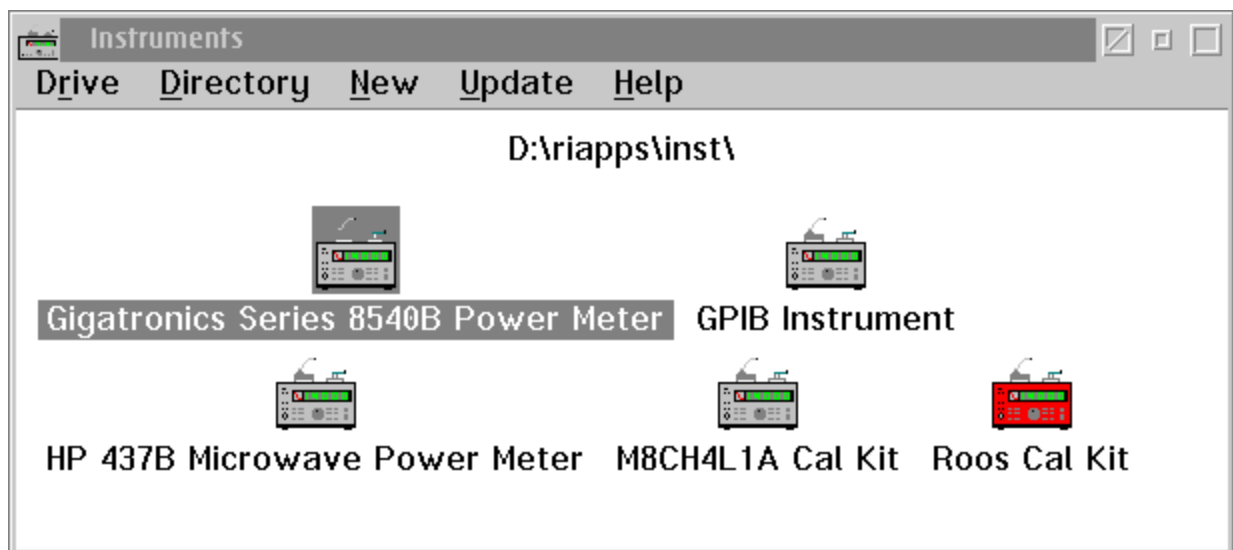


Figure 1
Available Instruments

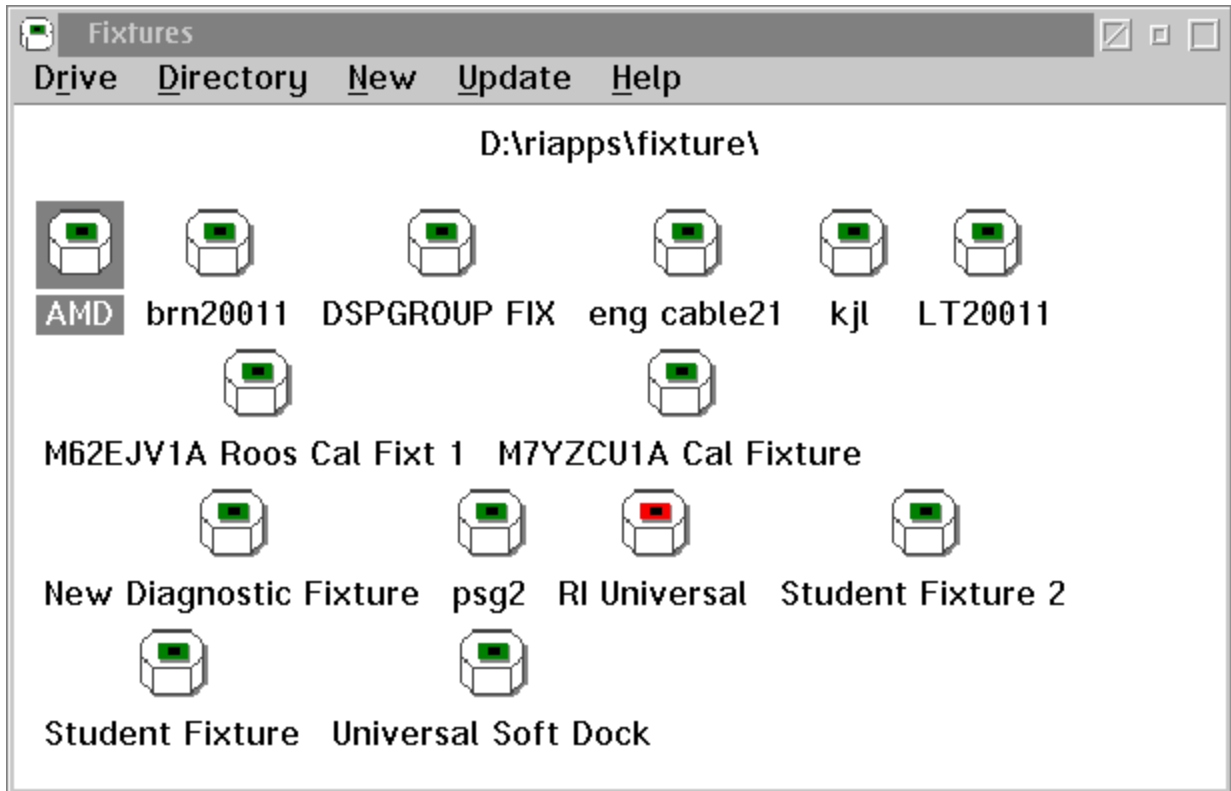


Figure 2
Fixtures

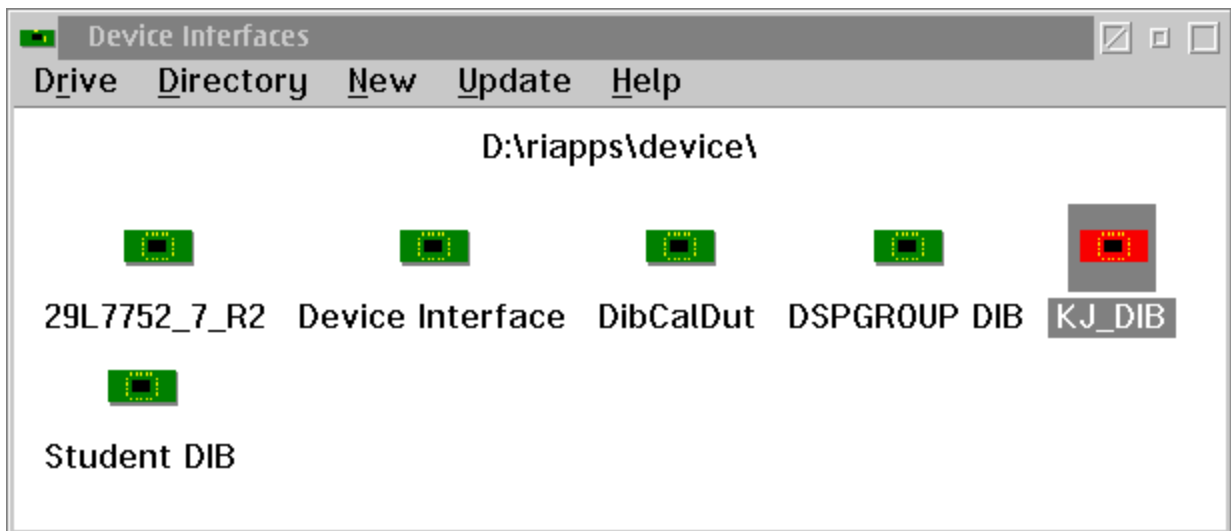


Figure 3
Device Interfaces

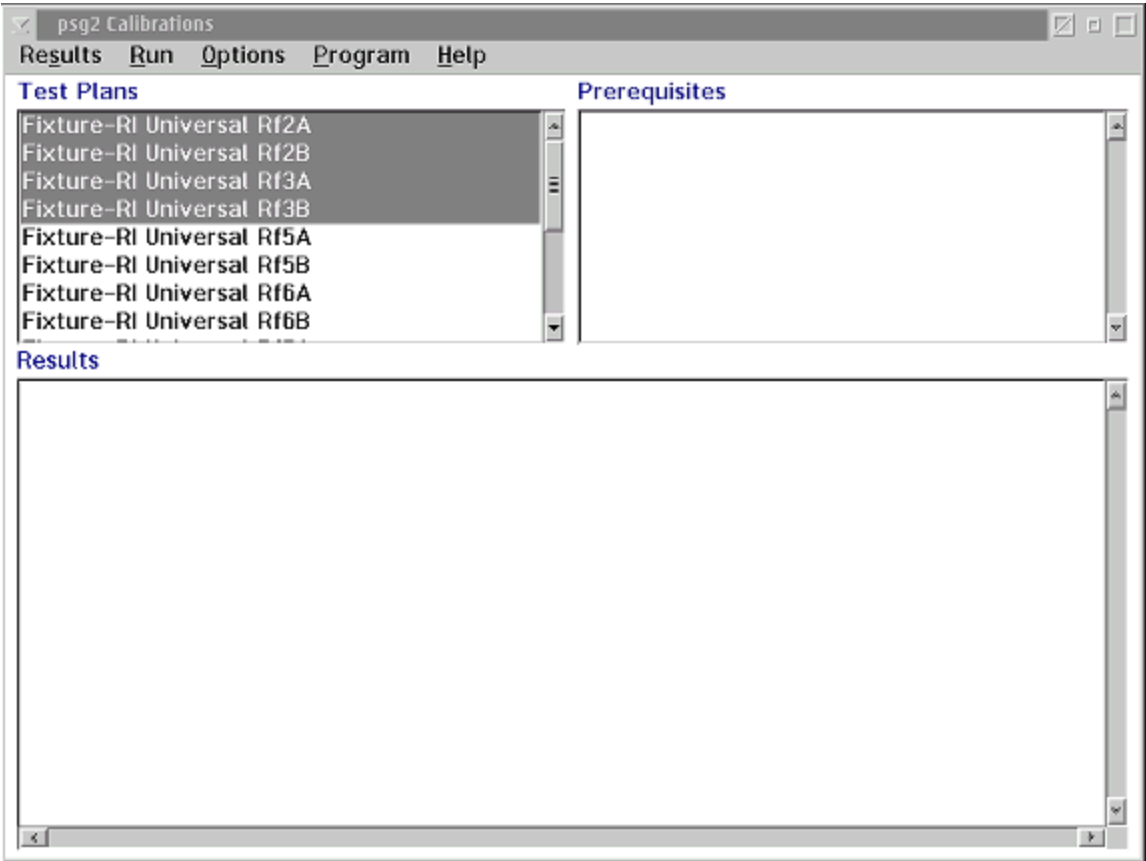


Figure 4
Calibrations

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Purpose: To give fixture users pointers on fixture maintenance and care.

Do's:

1. Store in a protected place when not in use such as a metal cabinet or book shelf.
2. Make sure that the shelf it sits on is clean. The installed standoffs will allow the fixture to sit without damage to the connectors.
3. Check DC and RF connections periodically to ensure good contact and that damage has not occurred.

Don'ts:

Store the fixture in such a way as to allow objects to contact the bottom surface. Anti-static styrofoam is OK. Doing otherwise may contribute to pin breakage, RF connector damage, or static discharge to sensitive DUT board components. Do not store on WIRE shelf racks.

Cleaning:

Periodic cleaning of the RF connectors and fixture in general is important. To clean the RF connectors, choose a good quality Q-tip or cotton swab. Wet the swab in Isopropyl alcohol. Then place the swab into the connector and twirl it once or twice only. To remove debris from the Teflon insert, use a tooth pick or other sharpened wood piece. Carefully wipe the insert being careful not to put pressure on the center conductor. Any dust or debris inside the fixture is best removed by a stream of compressed air.

Shipping:

In preparation to shipping the fixture the following steps should be noted.

1. Wrap the fixture in **two layers** of **anti-static** bubble material. The bubbles should have a diameter of no less than 0.8 inches. Styrofoam **should not** be used to protect pins during this process as it is a generator of static. Anti-static foam is OK.
2. Fill the box to be used for shipping half full of shipping peanuts. Use a box with dimensions of no less than 14" X 14" X 14".
3. Place the wrapped fixture into the box and finish filling it with shipping material and then seal it.

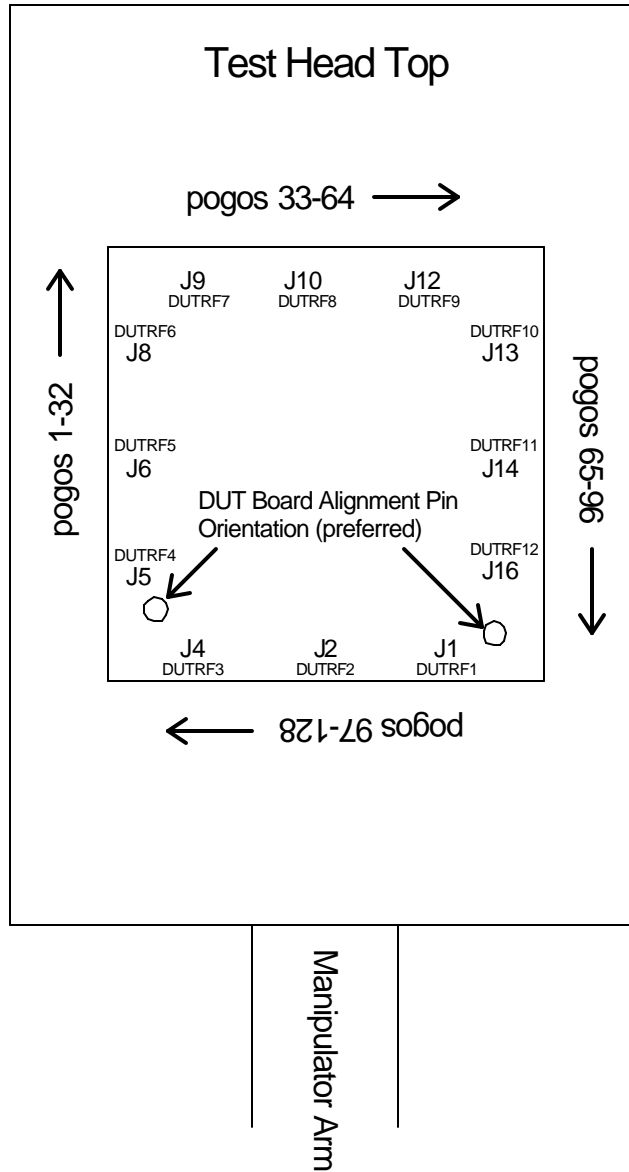
Fixture Carrier Board Pogo Alignment/Orientation

Revised: 12/12/2001 - 03/10/2003

Topic(s): Fixture

Doc ID:DFES-55CW2L

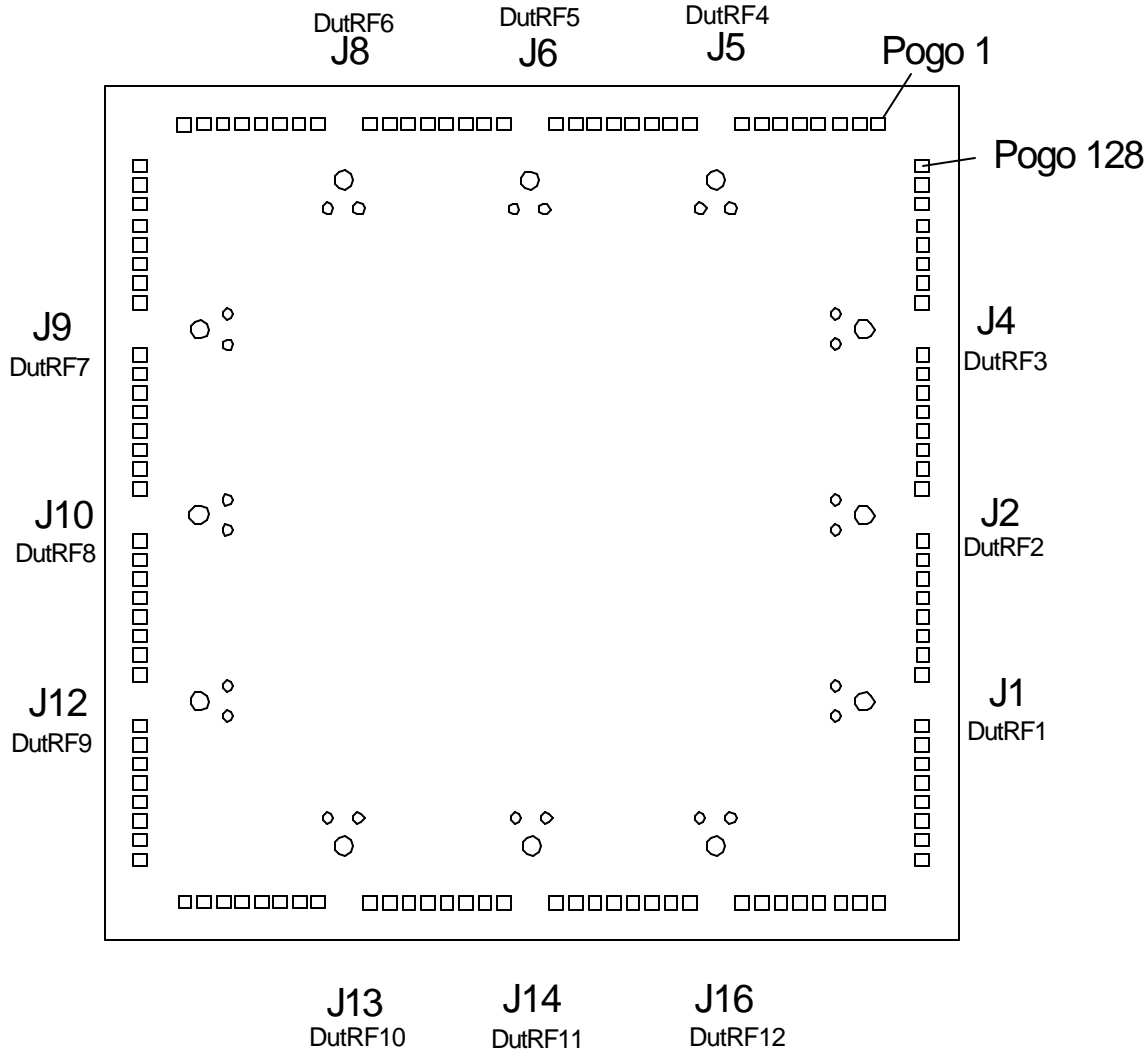
This document describes the fixture carrier board pogo orientation in relation to the test head. It can be used to orient Pin one (Pin 1) of the part to the Dut board nomenaclature.



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Fixture Training DIB Template (Bottom Side)





DIB Board Spread Sheet Training Example

PRODUCT	Training LNA/MIXER
DUT BOARD	
FIXTURE	Training

CARRIER BOARD PIN	CARRIER BOARD ID	RESOURCE	DUT PIN	NOTES / DUT PIN NAME
Dut RF12	J16			
Dut RF11	J14	RF3	5	MIXER RF XXXXXXXX0
Dut RF10	J13	RF7	6	MIXER IF XXXXXXXX0X
Dut RF9	J12			
Dut RF8	J10	RF2	7	MIXER LO
Dut RF7	J9			
Dut RF6	J8	RF3	8	AMP INPUT XXXXXXXX1
Dut RF5	J6			
Dut RF4	J5	RF7	3	AMP OUTPUT XXXXXXXX1X
Dut RF3	J4			
Dut RF2	J2			
Dut RF1	J1			

OTHER FROM	TO	NOTES / DUT PIN NAME
RF3	SW-MOD1-J6	Common Input of Switch Module SW 2
Carrier Bd - J14	SW-MOD1-J5	Normally Closed SW 2 XXXXXXXX0 Mixer input (RF)
Carrier Bd - J8	SW-MOD1-J4	Normally Open SW 2 XXXXXXXX1 Amp input
RF7	SW-MOD1-J3	Common Input of Switch Module SW 1
Carrier Bd - J13	SW-MOD1-J2	Normally Closed SW 1 XXXXXXXX0X Mixer output (IF)
Carrier Bd - J5	SW-MOD1_J1	Normally Open SW 1 XXXXXXXX1X Amp output
+5V	SW MOD1-H1-Pin8	
CBIT2	SW MOD1-H1-Pin6	
GND	SW MOD1-H1-Pin5	
CBIT1	SW MOD1-H1-Pin3	
-5V	SW MOD1-H1-Pin1	

CARRIER BOARD PIN	CARRIER BOARD ID	RESOURCE	DUT PIN	NOTES / DUT PIN NAME
P1	pogo 1			
P2				
P3				
P4				
P5				
P6				
P7				
P8		GND	4	GND
P9		GND		
P10	pogo 10	GNDREF		
P11				
P12		DP1	2	Vtest
P13		VCC5F	2	DUT VCC
P14		VCC5S	1	DUT VCC
P15				
P16				
P17	pogo 17			
P18				
P19				
P20		DB1		
P21				
P22				
P23				
P24				
P25		VII_F		
P26		VII_S		
P27		DB9		
P28				
P29				
P30				
P31				
P32				
P33				

CARRIER BOARD PIN	CARRIER BOARD ID	RESOURCE	DUT PIN	NOTES / DUT PIN NAME
P34				
P35				
P36				
P37				
P38				
P39				
P40		RTNS		
P41		VRTNS		
P42				
P43				
P44				
P45				
P46		VM1		
P47				
P48				
P49				
P50				
P51				
P52				
P53		VM2		
P54				
P55				
P56				
P57		DB2		
P58		DB3		
P59		DB4		
P60		DB5		
P61				
P62				
P63				
P64	pogo 64			
P65				
P66				

CARRIER BOARD PIN	CARRIER BOARD ID	RESOURCE	DUT PIN	NOTES / DUT PIN NAME
P67				
P68				
P69				
P70				
P71				
P72				
P73				
P74				
P75				
P76				
P77				
P78				
P79				
P80	pogo 80			
P81				
P82				
P83				
P84				
P85				
P86				
P87				
P88				
P89	pogo 89			
P90				
P91				
P92				
P93				
P94				
P95				
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P97				
P98				
P99				

CARRIER BOARD PIN	CARRIER BOARD ID	RESOURCE	DUT PIN	NOTES / DUT PIN NAME
P100				
P101				
P102				
P103				
P104				
P105				
P106	pogo 106			
P107				
P108				
P109				
P110				
P111	pogo 111			
P112		DP9		
P113		DP10		
P114				
P115				
P116				
P117				
P118	pogo 118			
P119				
P120				
P121				
P122				
P123				
P124				
P125				
P126				
P127				
P128				
RTNS (VI)	GND			

CARRIER BOARD PIN	CARRIER BOARD ID	RESOURCE	DUT PIN	NOTES / DUT PIN NAME
P1	pogo 1			
P2				
P3				
P4				
P5				
P6				
P7				
P8				
P9				
P10				
P11				
P12				
P13				
P14				
P15				
P16				
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CARRIER BOARD PIN	CARRIER BOARD ID	RESOURCE	DUT PIN	NOTES / DUT PIN NAME
P34				
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P40				
P41				
P42				
P43				
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P66				

CARRIER BOARD PIN	CARRIER BOARD ID	RESOURCE	DUT PIN	NOTES / DUT PIN NAME
P67				
P68				
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P73				
P74				
P75				
P76				
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CARRIER BOARD PIN	CARRIER BOARD ID	RESOURCE	DUT PIN	NOTES / DUT PIN NAME
P100				
P101				
P102				
P103				
P104				
P105				
P106				
P107				
P108				
P109				
P110				
P111				
P112				
P113				
P114				
P115				
P116				
P117				
P118				
P119				
P120				
P121				
P122				
P123				
P124				
P125				
P126				
P127				
P128				
RTNS (VI)	GND			



RiK0013A Carrier Board Interface Pin Designations

CB1	□	○	CB2	□	○
CB3	○	○	CB4	○	○
CB5	○	○	CB6	○	○
CB7	○	○	CB8	○	○
-5v	○	○	+5v	○	○
VRTN	○	○	-12V	○	○
+12V	○	○	+28V	○	○
S/N	○	○	SP	○	○
SP	○	○	SP	○	○
SP	○	○	SP	○	○
GND	○	○	DB9	○	○
DB10	○	○	DB11	○	○
DB12	○	○	DB13	○	○
DB14	○	○	DB15	○	○
DB16	○	○	GND	○	○
GND	○	○	DB1	○	○
DB2	○	○	DB3	○	○
DB4	○	○	DB5	○	○
DB6	○	○	DB7	○	○
GND	○	○	DB8	○	○

Connector side mapping 1:1

GND	□	○	VCC5F	□	○
VCC6F	○	○	VCC5S	○	○
VCC7F	○	○	VCC6S	○	○
VCC8F	○	○	VCC7S	○	○
GND	○	○	VCC8S	○	○
DP1	○	○	GRD	○	○
DP3	○	○	DP2	○	○
DP5	○	○	DP4	○	○
DP7	○	○	DP6	○	○
GND	○	○	DP8	○	○
DP9	○	○	GRD	○	○
DP11	○	○	DP10	○	○
DP13	○	○	DP12	○	○
DP15	○	○	DP14	○	○
GNDREF	○	○	DP16	○	○
VM1	○	○	GRD	○	○
VM2	○	○	VM1N	○	○
VM3	○	○	VM2N	○	○
VM4	○	○	VM3N	○	○
GND	○	○	VM4N	○	○

EDGE OF BOARD

Pin Designation Key:

- CB = Control Bits
- SP = Customer Specific/Undefined
- GND = Ground
- VRTN = Voltage Return
- DB = Static Digital
- VCC = Power Supply
- DP = Device Power
- GRD = Guard
- GNDREF = Ground Reference
- VMx = Voltage Measure x
- VM1N = Differential Voltage Measure x

