



# Agenda

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- New Capabilities
- New Fixture Modules
- New Calculations and New Buttons
- Local Variables and Disconnect Settings
- Using Connect Sequence & Pre/Post Measure Groups
- New Optimizer Capabilities
- I2C Read, Write, Extracting Data and Fixture Digital
- New Techniques for Modulated and/or Pulsed Signals



# New Capabilities

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- Fast Frequency Moves: 3x to 20x faster
- Low Current Measurements: down to <1 nA
- New High Speed ARB: up to 40 MHz Clock
- BER: up to 10 MHz
- RF Pulse Profiling: down to 100 nsec resolution
- IQ Meter: +/-0.1 deg. & +/-0.1 dB
- Fixture Digital: up to 60 Mbits/sec.
- High Current Pulse Measurements
- New Test Plan Optimizer Features: Show test times
- Digital Subsystem: 96 pins and 100 MHz Data rates



# New Fixture Modules

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- Low Frequency Noise Source: Noise to <1 MHz
- Delay Line Discriminator: Phase Noise Testing
- Attenuator Module: 3 to 33 dB attenuation, 2 dB steps
- Frequency Divider Module: Divide Ratios: 64, 128 & 256



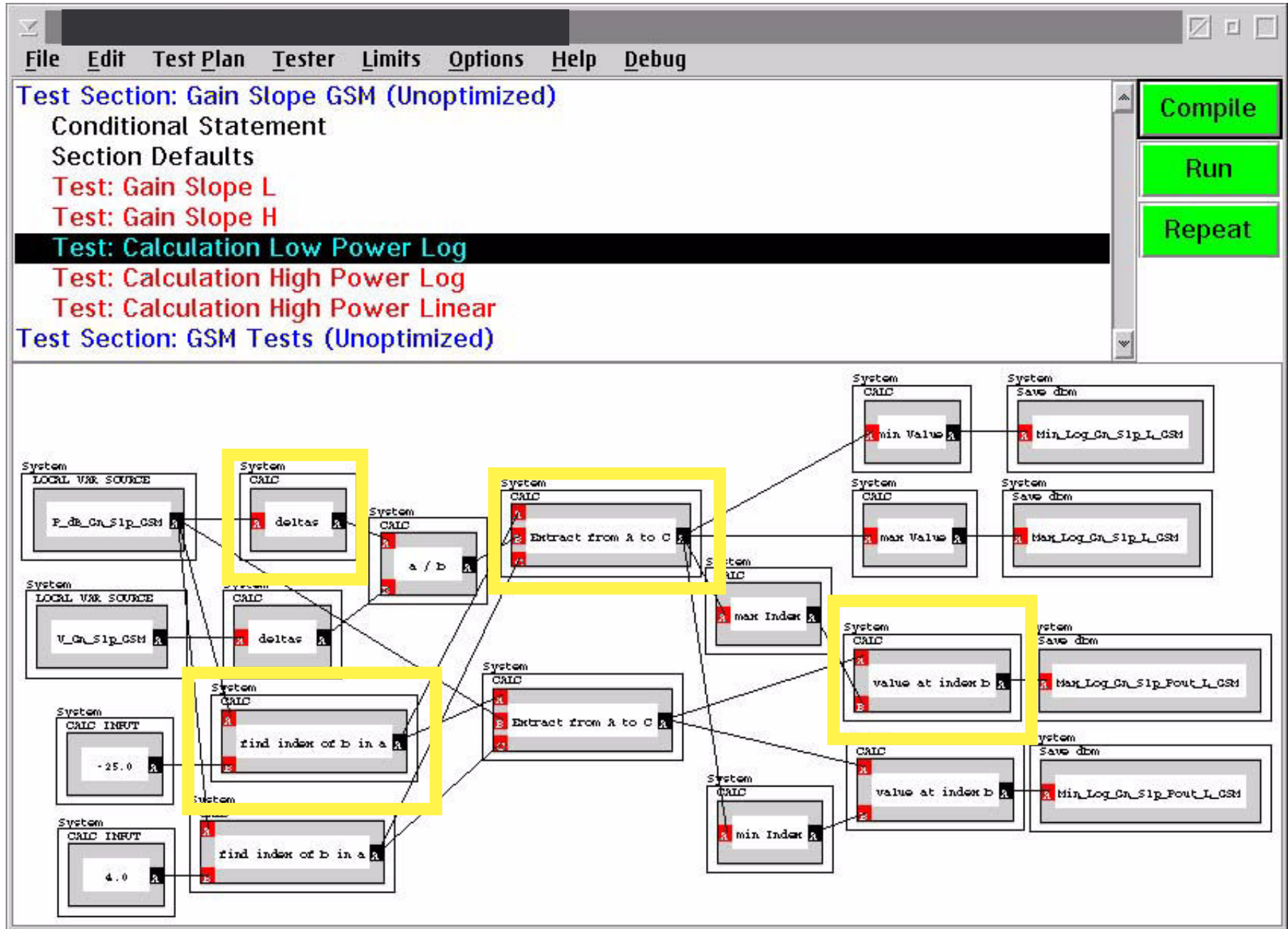
# New Calculations

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- Find index of b in a
- Value at index b
- Extract from A to C
- Deltas
- Modulo



# Calc Gain Slope using Deltas, Extract, Find Index & Value at Index



Test Section: A/D's Chk (Unoptimized)

Conditional Statement

Section Defaults

Test: A/D enable

Test: GPAD\_up\_pt1

Test: GPAD\_up\_pt2

Test: Test

Test: GPAD\_up\_pt3

Test: GPAD\_up\_pt4

Test: GPAD\_dn\_pt4

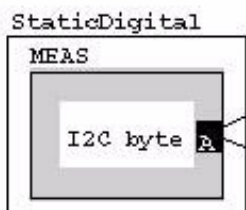
Test: GPAD\_dn\_pt3

Compile

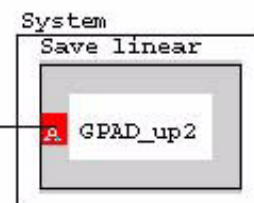
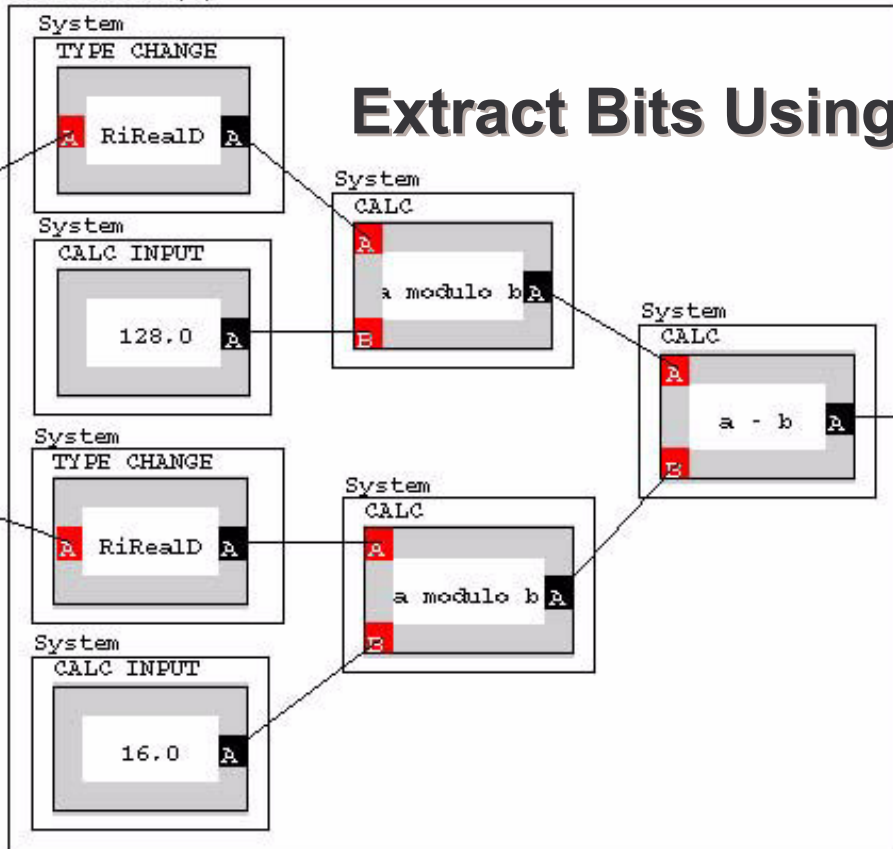
Run

Repeat

# Extract Bits Using Modulo Calc



## EXTRACT BIT(S)





# Global Defaults for Source 1, 2 & Receiver LO Fast Settle

The screenshot shows the 'Test Plan Settings' window with the 'Global Defaults' section selected. The interface includes a menu bar (File, Edit, Test Plan, Tester, Limits, Options, Help, Debug) and three green buttons on the right: 'Compile', 'Run', and 'Repeat'. The main area displays various configuration panels for different components:

- Aux Source:** Frequency (824 MHz), Power (-2 dBm), Modulation (CDMA), Src12Output Aux Power (-50 dBm).
- DutControl:** Device Power 1 (Vec 3), Device Power 2 (open), Vec 3 (2.85), Vec 4 (4.2).
- PowerVI:** Power V 1 (3.2), Power I 1 (2), V 1 Output (ON).
- Receiver:** FREQUENCY MASTER (Aux Source), CONFIG (Frequency), SCALE (1), OFFSET (0).
- Source1:** Fast Settle (ON), Src12Output Source 1 Attn (10db).
- Source2:** Frequency (824 MHz), Power (0 dBm), Rf State (OFF), Src12Output Source 1 Amp (ON), Src12Output (Aux + Src2 combined to src1), Fast Settle (ON).
- StaticDigital:** Voff (0), Von (2.8), Db 1 (off).
- System:** Freq Reference (Source2), Out Freq Offset (0), Out Freq Scale (1), Averages (8).
- Testhead:** Input Port (Rf 3), Output Port (Rf 6), Rf 3 (src1-noise), Rf 6 (receive), Rec Attenuation (30db), Source 1 (Rf 3), Parameter (b2).

A yellow box highlights the 'Fast Settle' controls for the Receiver (ON), Source 1 (ON), and Source 2 (ON).

# Global Default Setting for Src12Output: Aux + Src2 combined to Src1

The screenshot shows a software interface for configuring test plan settings. The top menu bar includes File, Edit, Test Plan, Tester, Limits, Options, Help, and Debug. The left sidebar lists various settings categories: Test Plan Settings, Global Defaults, Disconnect Settings, Connect Sequence, Test Section: DC Tests, Conditional Statement, Section Defaults, Test: lcc Idle High, and Test: lcc Idle Low. On the right side, there are three green buttons: Compile, Run, and Repeat. The main area displays a grid of settings for different components:

- Aux Source:** Frequency (824 MHz), Power (-2 dbm), Modulation (CDMA), Src12Output Aux Power (-50 dbm).
- DutControl:** Device Power 1 (Vec 3), Device Power 2 (open), Vec 3 (2.85), Vec 4 (4.2).
- PowerUI:** Power V 1 (3.2), Power I 1 (2), V 1 Output (ON).
- Receiver:** FREQUENCY MASTER (Aux Source), CONFIG (Frequency), SCALE (1), OFFSET (0), RecLo Fast Settle (ON).
- Source1:** Fast Settle (ON), Src12Output Source 1 Attn (10db).
- Source2:** Frequency (824 MHz), Power (0 dbm), Rf State (OFF), Src12Output Source 1 Amp (ON), Source2 Fast Settle (ON).
- StaticDigital:** Voff (0), Von (2.8), Db 1 (off).
- System:** Freq Reference (Source2), Out Freq Offset (0), Out Freq Scale (1), Averages (8).
- Testhead:** Input Port (Rf 3), Output Port (Rf 6), Rf 3 (src1-noise), Rf 6 (receive), Rec Attenuation (30db), Source 1 (Rf 3), Parameter (b2).

The **Src12Output** section is highlighted in yellow, showing the setting **Source Output Mode** set to **Aux + Src2 combined to src1**.





# Disconnect Settings Only

File Edit Test Plan Tester Limits Options Help Debug

Test Plan Settings  
Global Defaults  
**Disconnect Settings**  
Connect Sequence  
Test Section: GSM Transmit, LO Rejection, 4 points  
Conditional Statement  
Section Defaults  
Test: LO rejection, (+V,0)  
Test: LO rejection, (-V,0)  
Test: LO rejection, (0 +V)

Compile  
Run  
Repeat

Waveform

WF 2 Amplitude	WF 3 Amplitude
0	0
WF 2 Offset	WF 3 Offset
0	0
WF 2 Phase	WF 3 Phase
0	0

DutControl

Vcc 5
0

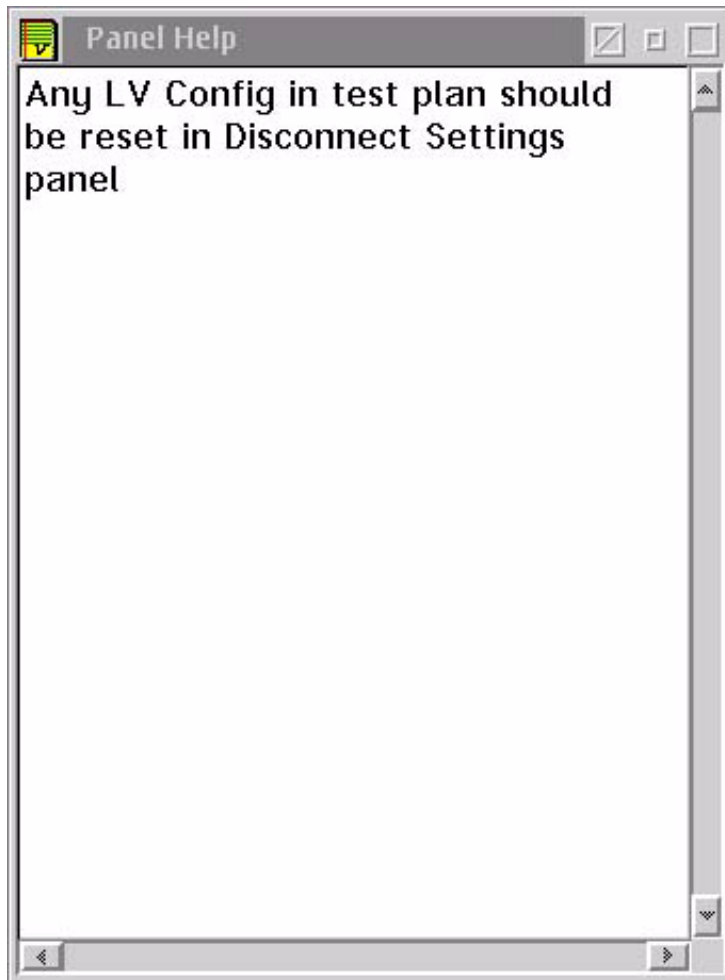
NOTE



# Disconnect Settings Panel

## Must include all Parameters set by Local Variable in Test Plan

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# Connect Sequence: Left to Right only

**Test Plan Settings**

- Global Defaults
- Disconnect Settings
- Connect Sequence**

**Test Section: Continuity Tests (Unoptimized)**

- Conditional Statement
- Section Defaults
- Test: Conn\_AGCOUT2
- Test: Conn\_AGCOUT1
- Test: Conn\_AGCCTR1

**Control Blocks:**

DutControl Device Power 1 Vcc 4	DutControl Device Power 2 Vcc 4	DutControl Device Power 3 Vcc 4	DutControl Device Power 4 Vcc 4	DutControl Device Power 5 Vcc 4	DutControl Device Power 6 Vcc 4	
DutControl Device Power 7 Vcc 4	DutControl Device Power 8 Vcc 3	DutControl Device Power 9 Vcc 2	DutControl Device Power 1 0 Vcc 2	DutControl Device Power 1 2 open	DutControl Device Power 1 3 open	
DutControl Device Power 1 4 open	DutControl Device Power 1 5 open	DutControl Device Power 1 6 open	DutControl Vcc 1 5	DutControl Vcc 2 5	DutControl Vcc 3 5	DutControl Vcc 4 5
DutControl Vcc 5 5	DutControl Vcc 6 5					

Test Section: lcc Normal (Unoptimized)

Conditional Statement

Section Defaults

Test: Reinit1

Test: lcc\_ina00

Test: lcc\_ina35

Test: lcc\_mix1

Test: lcc\_vga\_norm35

Test: lcc\_vga\_hi35

Test: lcc\_mix2fga\_norm

Test: lcc\_mix2fga\_hi

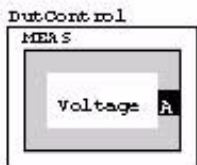
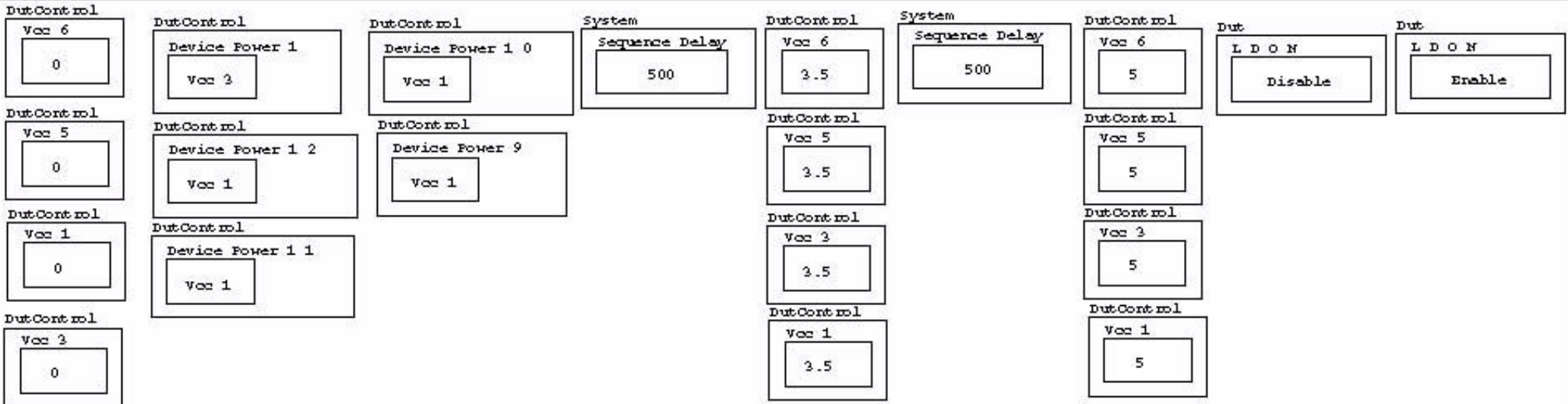
Compile

Run

Repeat

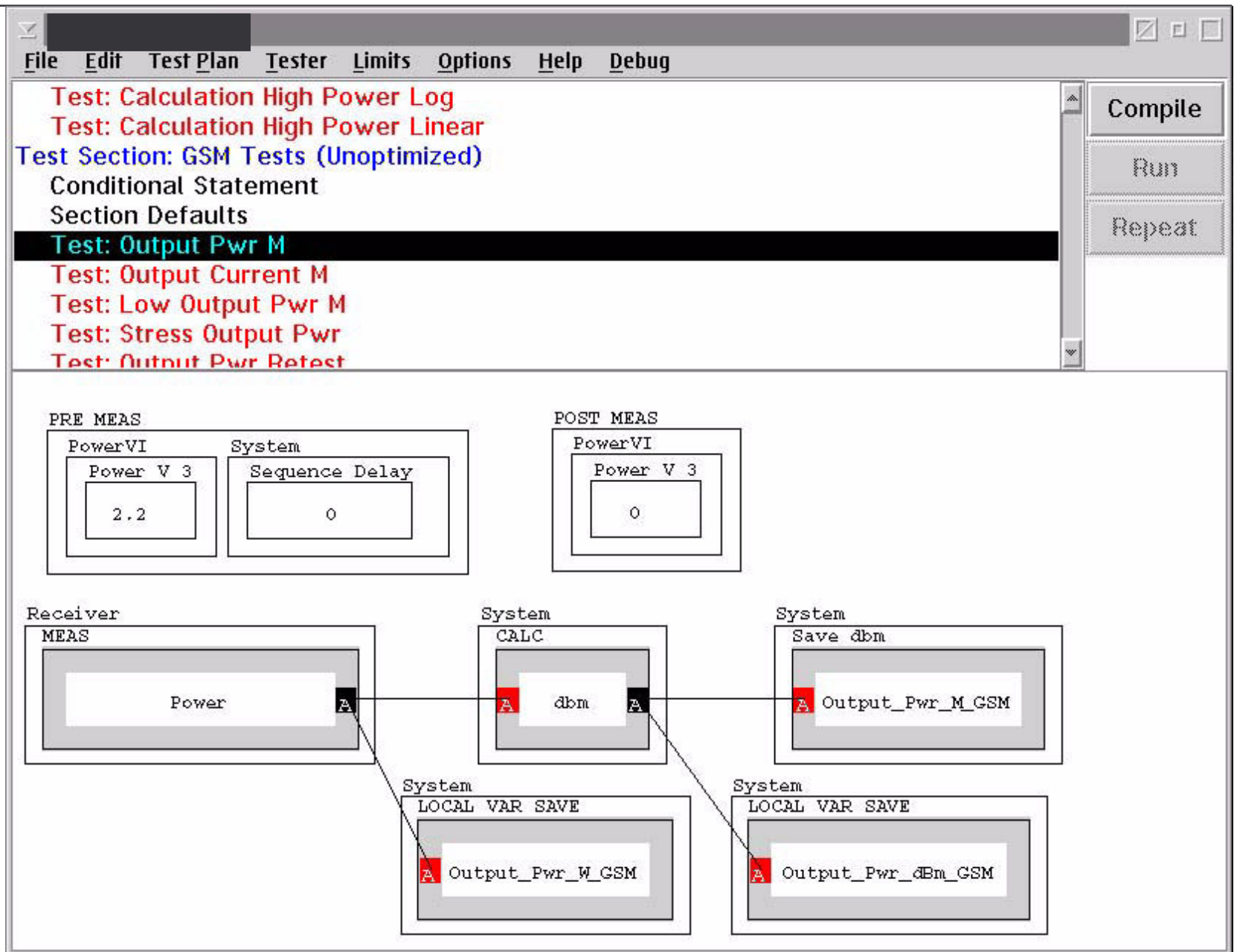
# PreMeasure Sequence Left to Right only

PRE MEAS





# GSM Pulse Sequence, Pulse Voltage and Measure Power Using Pre Measure and Post Measure Groups





# Optimizer: Optimizes over each Test Section. Compiled Delta Settings Shows Test Times

The screenshot shows a software window titled "Test Plan Settings". The left pane lists test sections and their steps:

- Testplan idle Settings
- Section: DC Tests
  - 1. Icc Power Down (Current)
  - 2. Icc Idle High (Current)
  - 3. Icc Idle Low (Current)
- Section: 824 MHz AMPS FH1 Fine
  - 1. AMPS Sweep (RelativeVc)
  - 2. AMPS Sweep (RelativeVc)
  - 3. AMPS Sweep (RelativeVc)
  - 4. AMPS Sweep (RelativeVc)
  - 5. AMPS Sweep (RelativeVc)
- Section: 824 MHz AMPS FE1 Fine
  - 1. AMPS Sweep (RelativeVc)
  - 2. AMPS Sweep (RelativeVc)
  - 3. AMPS Sweep (RelativeVc)
  - 4. AMPS Sweep (RelativeVc)
  - 5. AMPS Sweep (RelativeVc)
- Section: 824 MHz AMPS FH1 Out
  - 1. Power Gain FH1 (Relative)
  - 2. Operating Current FH1 (C)
- Section: 824 MHz AMPS FE1 Out
  - 1. Power Efficiency FE1 (Re)
  - 2. Operating Current FE1 (C)
- Section: 824 MHz CDMA HP Find
  - 1. CDMA HP Sweep (Relativ)
  - 2. CDMA HP Sweep (Relativ)
  - 3. CDMA HP Sweep (Relativ)
  - 4. CDMA HP Sweep (Relativ)
  - 5. CDMA HP Sweep (Relativ)
  - 6. CDMA HP Sweep (Relativ)

The right pane displays hardware timing data, highlighted with a yellow box:

```
Total Testplan Hardware timing
Setup pauses 80435.2 us
Setup Settling Time 220400 us
TOTAL Setup Time 321153.3 us
Measure pauses 264596.8 us
TOTAL Meas Time 379283.0 us
Total Hardware Test Time 700436.3 us
**Deltas*****
```



# Optimizer: Optimizes each Test Section. Lowest DUT Frequency Measured First

The screenshot displays a software interface with a list of test sections on the left and their configuration details on the right. The sections are:

- Section: 824 MHz CDMA ACPr M...
  1. Alternate Low HP (RelativeVoltageVsTime)
  2. Adjacent Low HP (RelativeVoltageVsTime)
  3. Adjacent High HP (RelativeVoltageVsTime)
  4. Alternate High HP (RelativeVoltageVsTime)
  5. Alternate Low LP (RelativeVoltageVsTime)
  6. Adjacent Low LP (RelativeVoltageVsTime)
  7. Adjacent High LP (RelativeVoltageVsTime)
  8. Alternate High LP (RelativeVoltageVsTime)
- Section: 824 MHz AMPS Harmonic...
  1. 2nd Harmonic FE1 (RelativeVoltageVsTime)
  2. 3rd Harmonic FE1 (RelativeVoltageVsTime)
- Section: 849 MHz CDMA HP Find...
  1. CDMA HP Sweep (RelativeVoltageVsTime)
  2. CDMA HP Sweep (RelativeVoltageVsTime)
  3. CDMA HP Sweep (RelativeVoltageVsTime)
  4. CDMA HP Sweep (RelativeVoltageVsTime)
  5. CDMA HP Sweep (RelativeVoltageVsTime)
  6. CDMA HP Sweep (RelativeVoltageVsTime)
- Section: 849 MHz CDMA Output...
  1. Channel Power (RelativeVoltageVsTime)
  2. Prefl\_RL (RelativeRms)
  3. Operating Current (Current)
  4. Pin (RelativeRms)
- Section: 849 MHz CDMA LP Find...
  1. CDMA LP Sweep (RelativeVoltageVsTime)
  2. CDMA LP Sweep (RelativeVoltageVsTime)
  3. CDMA LP Sweep (RelativeVoltageVsTime)
  4. CDMA LP Sweep (RelativeVoltageVsTime)
  5. CDMA LP Sweep (RelativeVoltageVsTime)
  6. CDMA LP Sweep (RelativeVoltageVsTime)

The configuration details for the first section are:

```
1. Alternate Low HP (RelativeVoltageVsTime) Hardware time
Setup pauses 318.4 us
Setup Settling Time 5000 us
TOTAL Setup Time 6049.0 us
Measure pauses 752.6 us
TOTAL Meas Time 2242.6 us
Total Hardware Test Time 8291.6 us
**Deltas*****
Receiver
  FreqOffset -- RiFreqD(-1.98 )
  IfBw --> narrow
  IfGain --> 56
RecLo
  FreqOffset --> -1.98
Src12Output
  AuxPower --> 824_CDMA_HP_AuxPwrSet_28
StaticDigital
  CurrentMeasMax --> RiCurrentD(1.0 )
  Db1 --> off
  MeasureLimit --> RiCurrentD(0.0 )
  MeasureMode --> none
  MeasurePin --> none
  MeasureVForce --> RiVoltageD(0.0 )
System
  Averages --> 16
Testhead
  RecAttenuation --> 20
```



# Optimizer: Optimizes each Test Section. Measurement with Lowest Input Power Performed First

**Test Plan Settings**

Testplan idle Settings

**Section: DC Tests**

1. Icc Power Down (Current)
2. Icc Idle High (Current)
3. Icc Idle Low (Current)

**Section: 824 MHz AMPS FH1 Find**

1. AMPS Sweep (RelativeVc)
2. AMPS Sweep (RelativeVc)
3. AMPS Sweep (RelativeVc)
4. AMPS Sweep (RelativeVc)
5. AMPS Sweep (RelativeVc)

**Section: 824 MHz AMPS FE1 Find**

1. AMPS Sweep (RelativeVc)
2. AMPS Sweep (RelativeVc)
3. AMPS Sweep (RelativeVc)
4. AMPS Sweep (RelativeVc)
5. AMPS Sweep (RelativeVc)

**Section: 824 MHz AMPS FH1 Out**

1. Power Gain FH1 (Relative)
2. Operating Current FH1 (C)

**Section: 824 MHz AMPS FE1 Out**

1. Power Efficiency FE1 (Re)
2. Operating Current FE1 (C)

**Section: 824 MHz CDMA HP Find**

1. CDMA HP Sweep (Relativ
2. CDMA HP Sweep (Relativ
3. CDMA HP Sweep (Relativ
4. CDMA HP Sweep (Relativ
5. CDMA HP Sweep (Relativ
6. CDMA HP Sweep (Relativ

1. CDMA HP Sweep (RelativeRms) Hardware timing

Setup pauses 24.0 us

Setup Settling Time 100 us

TOTAL Setup Time 222.2 us

Measure pauses 5754.7 us

TOTAL Meas Time 7374.7 us

Total Hardware Test Time 7596.9 us

**\*\*Deltas\*\*\*\*\***

PowerV1

PowerV1 -- RiVoltageD(3.2 )

Source2

Power --> RiPowerDbm(0.0 )

RfState --> off

Src12Output

AuxPower --> RiPowerDbm(-26.0 )

System

Averages --> 16





# Static Digital Settings for Continuity Test: Set Current Measure Voltage

The screenshot shows a software window with a menu bar (File, Edit, Test Plan, Tester, Limits, Options, Help, Debug) and a list of tests under the heading "Test Section: Continuity Tests (Unoptimized)". The test "Test: Conn\_AGCOUT2" is selected. Below the list, several configuration boxes are displayed:

- StaticDigital Measure Pin:** DB12
- StaticDigital Db 1 2:** open
- StaticDigital Measure I Force:** -200 u
- StaticDigital Measure I Limit:** -200 u
- StaticDigital Measure Mode:** vMeas
- StaticDigital Measure V Limit:** -1.5
- StaticDigital MEAS:** Voltage A
- System Save Volts:** A AGCOUT2\_conn

A line connects the "A" in the MEAS box to the "A" in the Save Volts box.



# Static Digital Settings for Leakage Test Set Voltage, Measure Current

**File Edit Test Plan Tester Limits Options Help Debug**

**Test: Conn\_MIX2VCCrf**  
**Test Section: Leakage Biased (Unoptimized)**  
Conditional Statement  
Section Defaults  
**Test: Leak\_AGCCTRL\_Biased**  
**Test: Leak\_A1\_Biased**  
**Test: Leak\_A2\_Biased**  
**Test: Leak\_I2CCLK\_Biased**  
**Test: Leak\_AFCin\_Biased**  
**Test Section: I2C Defaults Read Tests (Unoptimized)**

**Compile**  
**Run**  
**Repeat**

StaticDigital Measure Mode: Imeas  
StaticDigital Measure Pin: DB3  
StaticDigital Db 3: open  
StaticDigital Measure V Force: 0  
StaticDigital Current Meas Max: 20 u  
StaticDigital Measure I Limit: 20 u

StaticDigital MEAS: Current A  
System Save Amps: I2CCLK\_leak\_Biased  
System Pause: 10000

Test: lcc\_vcc  
Test: lcc\_total\_shdn  
Test Section: I2C Read Defaults / Dev. Addr (Unoptimized)  
Conditional Statement  
Section Defaults  
Test: Reset\_I2C  
**Test: Reg00**  
Test: Reg01  
Test: Reg02  
Test: Reg03  
Test: Reg04

Compile  
Run  
Repeat

StaticDigital  
I 2 C Address  
1100000

StaticDigital  
I 2 C Register  
00000000

## Set I2C Address & Register, Perform I2C Read and Save Byte

StaticDigital  
Db 1 1  
off

StaticDigital  
MEAS  
I2C byte A

System  
Save linear  
A Reg00





File Edit Test Plan Tester Limits Options Help Debug

Test Section: DC Test @ Normal mode (Unoptimized)

Conditional Statement  
Section Defaults  
Test: Icc\_UPCVCC  
Test: Icc\_MIX2VCCrf  
Test: Icc\_IFVCC  
Test: Icc\_L01\_I2C\_SR0  
Test: Icc\_L02\_VGA  
Test: Icc\_Normal\_mode  
Test: Icc\_UPCVCC\_psm1

Compile  
Run  
Repeat

Dut System

U P B U F I  
2  
Pause  
2000

### I2C Write to DUT & Measure Icc

DutControl System

MEAS Save Amps

Current A Icc\_UPCVCC\_psm1

Current Meas Max  
0.125

Imeasure  
Vcc5

The screenshot shows a software interface for configuring a test. The top part is a menu bar with 'File', 'Edit', 'Test Plan', 'Tester', 'Limits', 'Options', 'Help', and 'Debug'. Below is a 'Test Section: DC Test @ Normal mode (Unoptimized)' with a list of tests. The last test, 'Icc\_UPCVCC\_psm1', is highlighted. To the right are 'Compile', 'Run', and 'Repeat' buttons. The main area contains a block diagram with 'Dut' and 'System' blocks. The 'Dut' block has a 'UPBUI' section with a value of '2'. The 'System' block has a 'Pause' section with a value of '2000'. Below this is another 'DutControl' and 'System' block. The 'DutControl' block has a 'MEAS' section with 'Current A' and 'Current Meas Max' (0.125), and an 'Imeasure' section with 'Vcc5'. The 'System' block has a 'Save Amps' section with 'Icc\_UPCVCC\_psm1'. A line connects the 'Current A' measurement point to the 'Save Amps' block.

Test Section: A/D's Chk (Unoptimized)

Conditional Statement

Section Defaults

Test: A/D enable

Test: GPAD\_up\_pt1

Test: GPAD\_up\_pt2

Test: Test

Test: GPAD\_up\_pt3

Test: GPAD\_up\_pt4

Test: GPAD\_dn\_pt4

Test: GPAD\_dn\_pt3

Compile

Run

Repeat

## PreMeasure & Multiple I2C Buttons

PRE MEAS

Dut

V A D E

Disable

Dut

G P S D

SHDN gpad

Dut

V A D E

Enable

Dut

G P S D

Idle

DutControl

MEAS

Voltage A



File Edit Test Plan Tester Limits Options Help Debug

Test Section: AFC ADC Tests (Unoptimized)  
Conditional Statement  
Section Defaults  
Test: ADC\_Vts  
Test: ADC\_disable

Test Section: L01 ADC tests (Unoptimized)  
Conditional Statement  
Section Defaults  
Test: L01\_disable  
Test: L01reg\_init

Compile  
Run  
Repeat

## I2C Write, Read & Modulo Calculation

Dut  
A F Cen  
disable

StaticDigital  
Von High Byte  
3.2

StaticDigital  
MEAS  
IC byte

System  
TYPE CHANGE  
RiRealD

System  
TYPE CHANGE  
RiRealD

System  
CALC INPUT  
8.0

System  
CALC  
a modulo b

System  
CALC INPUT  
0.0

System  
CALC  
a modulo b

System  
CALC  
a - b

System  
Save linear  
ADC\_Vt\_disable

Test Section: A/D's Chk (Unoptimized)

Conditional Statement

Section Defaults

Test: A/D enable

Test: GPAD\_up\_pt1

Test: GPAD\_up\_pt2

Test: Test

Test: GPAD\_up\_pt3

Test: GPAD\_up\_pt4

Test: GPAD\_dn\_pt4

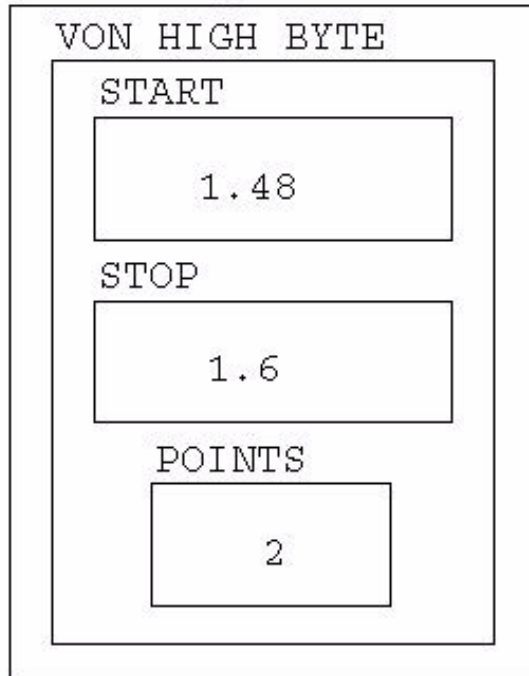
Test: GPAD\_dn\_pt3

Compile

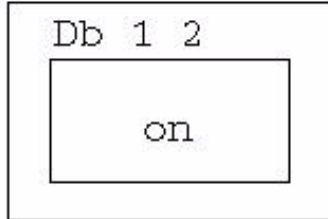
Run

Repeat

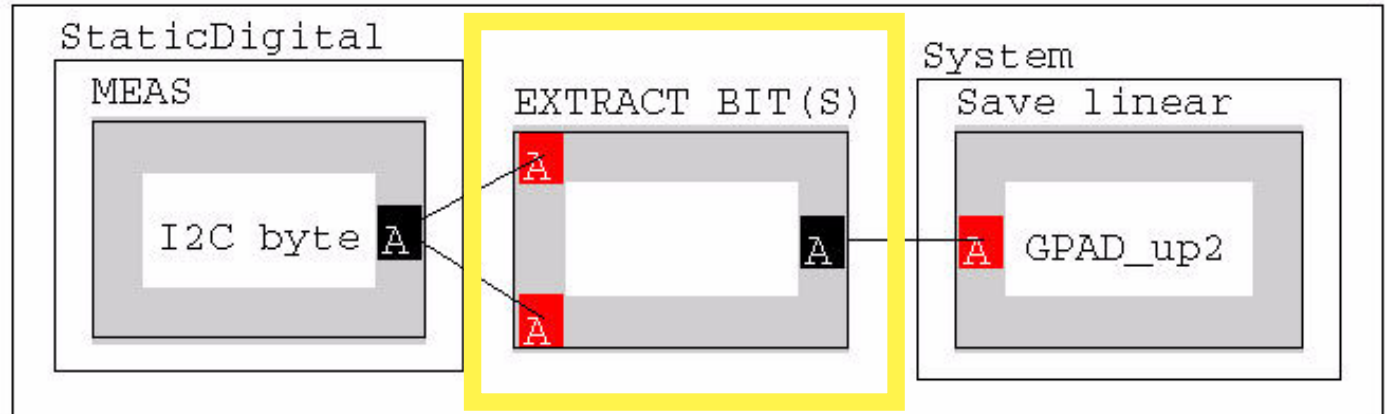
StaticDigital



StaticDigital



## I2C Read and Extract Bits



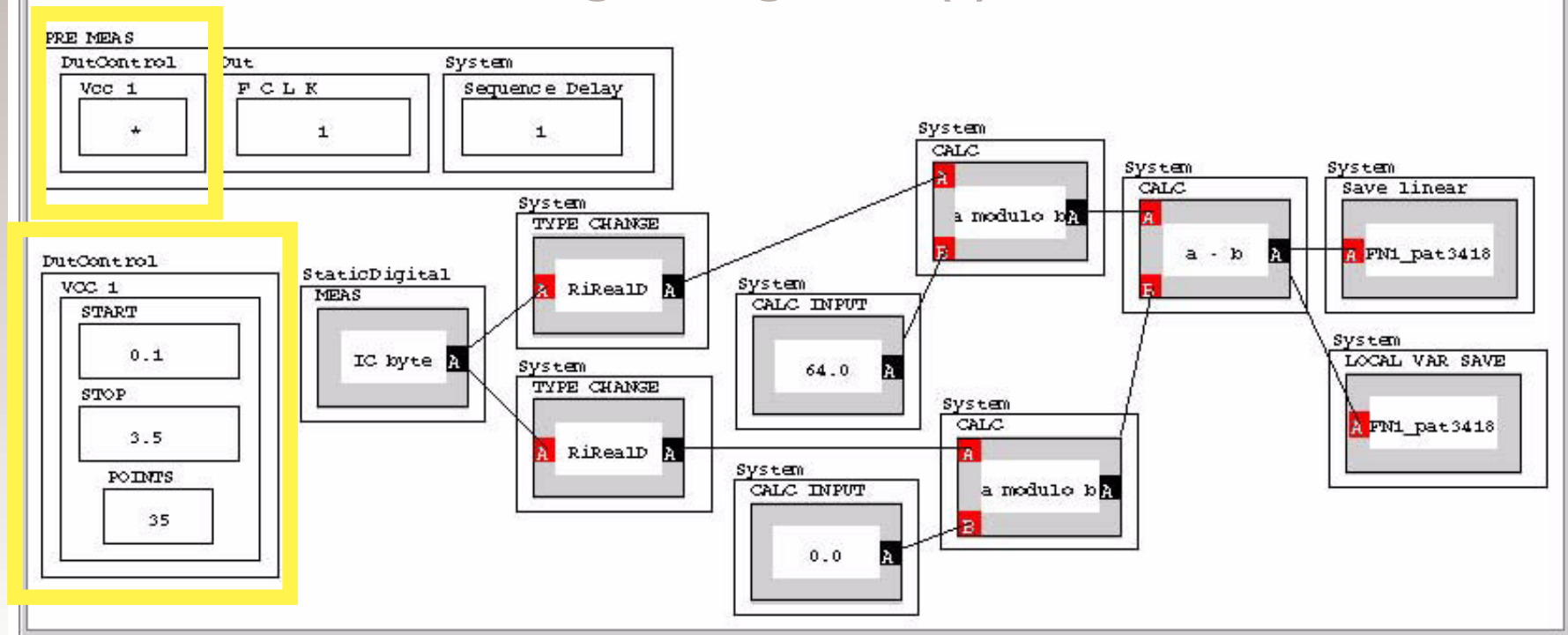


File Edit Test Plan Tester Limits Options Help Debug

Test: I2PIND\_test@GC15@AGC\_3.0V  
Test Section: FN1\_testmode (Unoptimized)  
Conditional Statement  
Section Defaults  
Test State: FN1\_pattern1  
Test: FN1\_pat3418\_init1  
Test: FN1\_pat3418\_init2  
Test: FN1\_pat3418\_init3  
Test: CleanFN1\_3418  
Test: FN1\_pat3418

Compile  
Run  
Repeat

## Fractional N Testing Using Vcc1(\*)





Test Section: FracN testmode (Unoptimized)

Conditional Statement

Section Defaults

Test: FN2 Test init

Test: FN2 Test6836

Test: FN2 Test init1

Test: FN2 Test init2

Test: FN2 Test2020

Test: FN2 Test init1

Test: FN2 Test init2

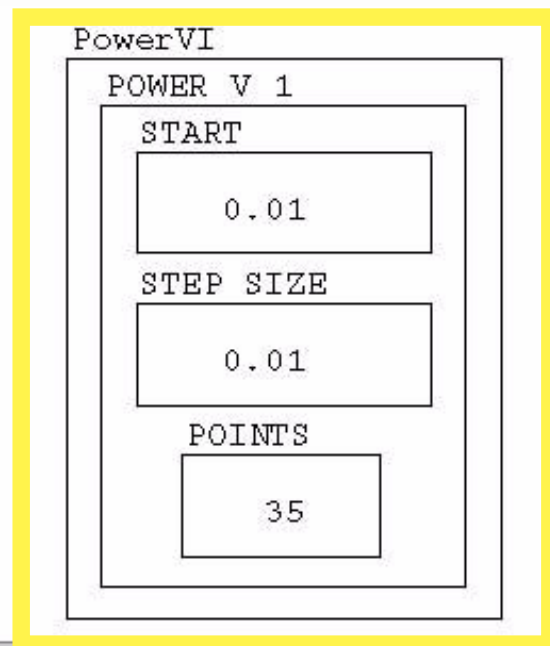
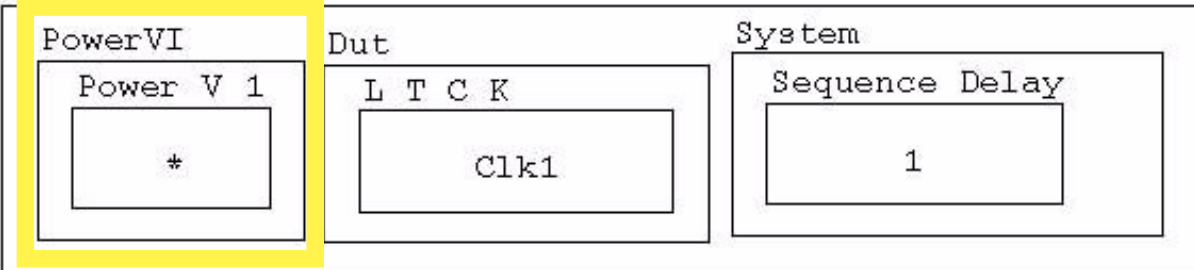
Test: FN2 Test1354

Compile

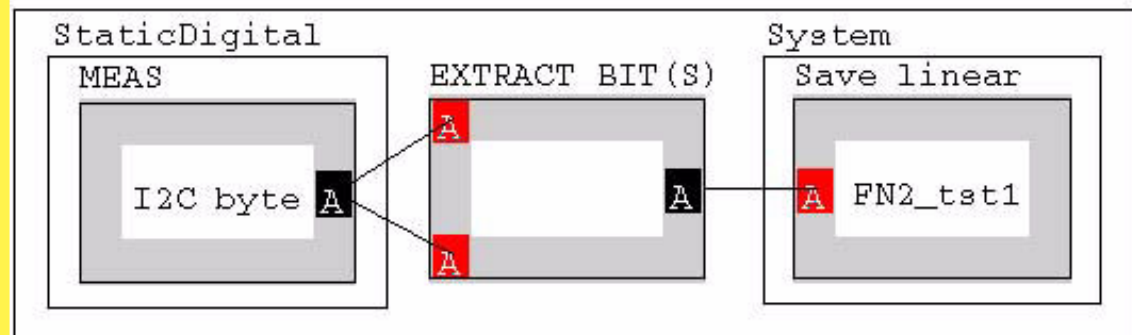
Run

Repeat

PRE MEAS



### Clocking I2C Bit using VI1(\*)



# Fixture Digital Default Settings

File Edit Test Plan Tester Limits Options Help Debug

Test Plan Settings

- Global Defaults
- Disconnect Settings
- Connect Sequence
- Test Section: Continuity (Unoptimized)
- Conditional Statement
- Section Defaults

Compile

Run

Repeat

FixtureDigital Wall 0.5	FixtureDigital Wall 2	FixtureDigital Db 1 off	FixtureDigital Db 2 off	FixtureDigital Db 3 on	FixtureDigital Vector Type Format 1	FixtureDigital Serial Type DUT	FixtureDigital Drive Mask 0000444	FixtureDigital Vector Clock Period 20 n
PowerM Power L 1 0.1	OutControl Vec 6 5	State Digital Serial Clock Period 400 n	Receiver Frequency 30 Mhz	Source 1 Frequency 30 Mhz	Source 2 Frequency 200 Mhz	Source 3 Frequency 300 Mhz	State Digital Db 6 Db2	
OutControl Device Power 1 6 Vec 2	Fixture Head R14 DutR14	Fixture Head R15 DutR15	Receiver Input .005 - 2 Input	Power -20 dbm	Power -23 dbm	Power -100 dbm	State Digital Clock Db3	
OutControl Device Power 1 Vec 4	OutControl Vec 2 5	Testhead Input Port R15	Receiver ILGain 50	RI Slack ON	RI Slack OFF	RI Slack OFF	State Digital Strobe 1 Db7	
OutControl Device Power 2 open	OutControl Vec 4 5	Output Port R14	Receiver ILBW 4 Mhz	Src BOutput Source 1 A1n 30db	Src BOutput Source 2 A1n 30db	System Averages 15	State Digital Wall 0.5	
Dut Tx_En Tx_En	Gain 63	State Digital Db 5 on	State Digital Db 5 on	Testhead Source 1 RF 5	Src BOutput Source 1 Output Mode low band	Fixture Fixture Power ON	State Digital Wall 2	State Digital Serial Type None

NOTE



# Fixture Digital Leakage Current

**Test: Conn\_Vout**  
**Test: DiodeTxen\_meas**  
**Test: DiodeSHDN\_meas**  
**Test: DiodeCS\_meas, CS is DB7**  
**Test Section: Leakage, need to change I\_Limit from -50 nA to -1000 nA (Unoptimized)**  
**Conditional Statement**  
**Section Defaults**  
**Test: Leakage\_CS, CS is DB7, changed premeasure sequence**  
**Test: Leakage\_SDA, changed to DB2, changed premeasure sequence**

**PRE MEAS**

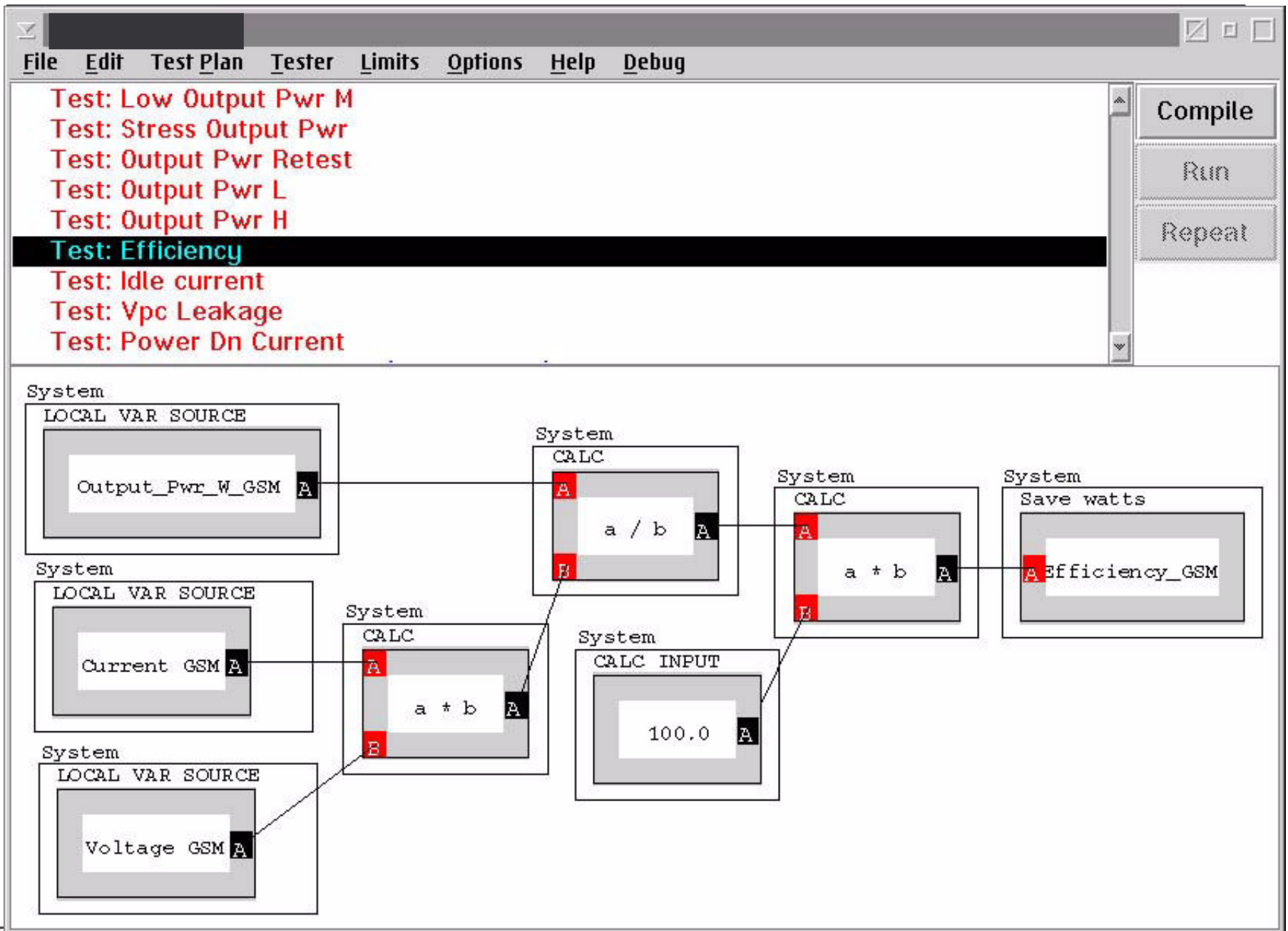
- StaticDigital Measure Pin**: DB7
- System Sequence Delay**: 1000
- FixtureDigital Db 1**: open

**MEAS**

- StaticDigital MEAS**: Current A
- System Save linear**: A Leaki\_SDA
- FixtureDigital Measure Pin**: DB1

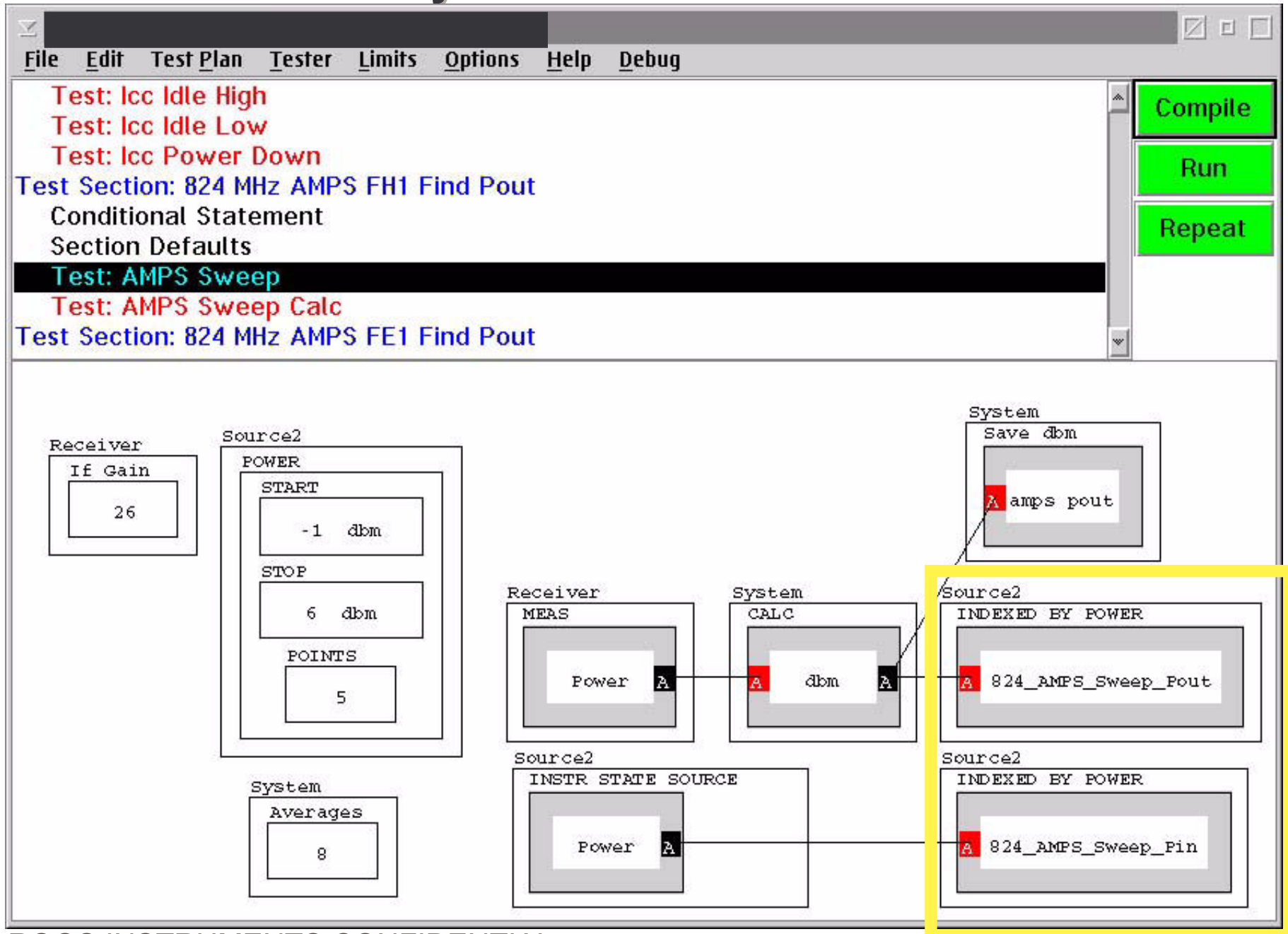


# PAE: Power Added Efficiency





# Sweep Pin, Measure Pout, Save Pin and Pout Data in Local Variables indexed by Source 2 Power





# Calculate Pin such that Pout is +31 dBm

File Edit Test Plan Tester Limits Options Help Debug

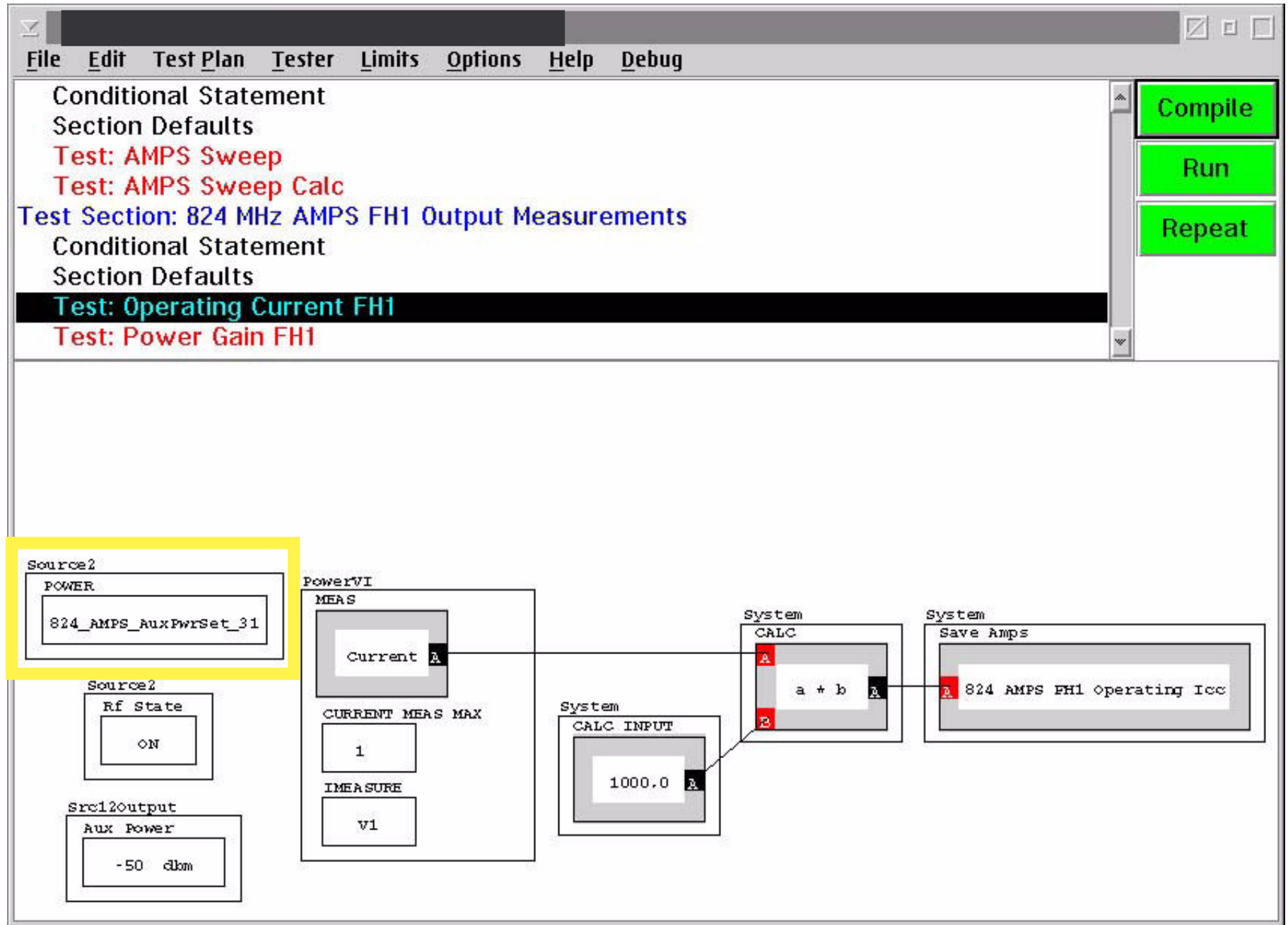
Test: Icc Idle High  
Test: Icc Idle Low  
Test: Icc Power Down  
Test Section: 824 MHz AMPS FH1 Find Pout  
Conditional Statement  
Section Defaults  
Test: AMPS Sweep  
**Test: AMPS Sweep Calc**  
Test Section: 824 MHz AMPS FE1 Find Pout

Compile  
Run  
Repeat

```
graph LR; LVS1[System LOCAL VAR SOURCE 824_AMPS_Sweep_Pout] --> C1[System CALC find index of b in a]; C1 --> C2[System CALC value at index b]; C2 --> LVS2[System LOCAL VAR SAVE 824_AMPS_AuxPwrSet_31]; LVS2 --> S[System Save dbm 824_AMPS_Pin_Set_31]; CIP[System CALC INPUT 31.0] --> C1; LVS3[System LOCAL VAR SOURCE 824_AMPS_Sweep_Pin] --> C2;
```

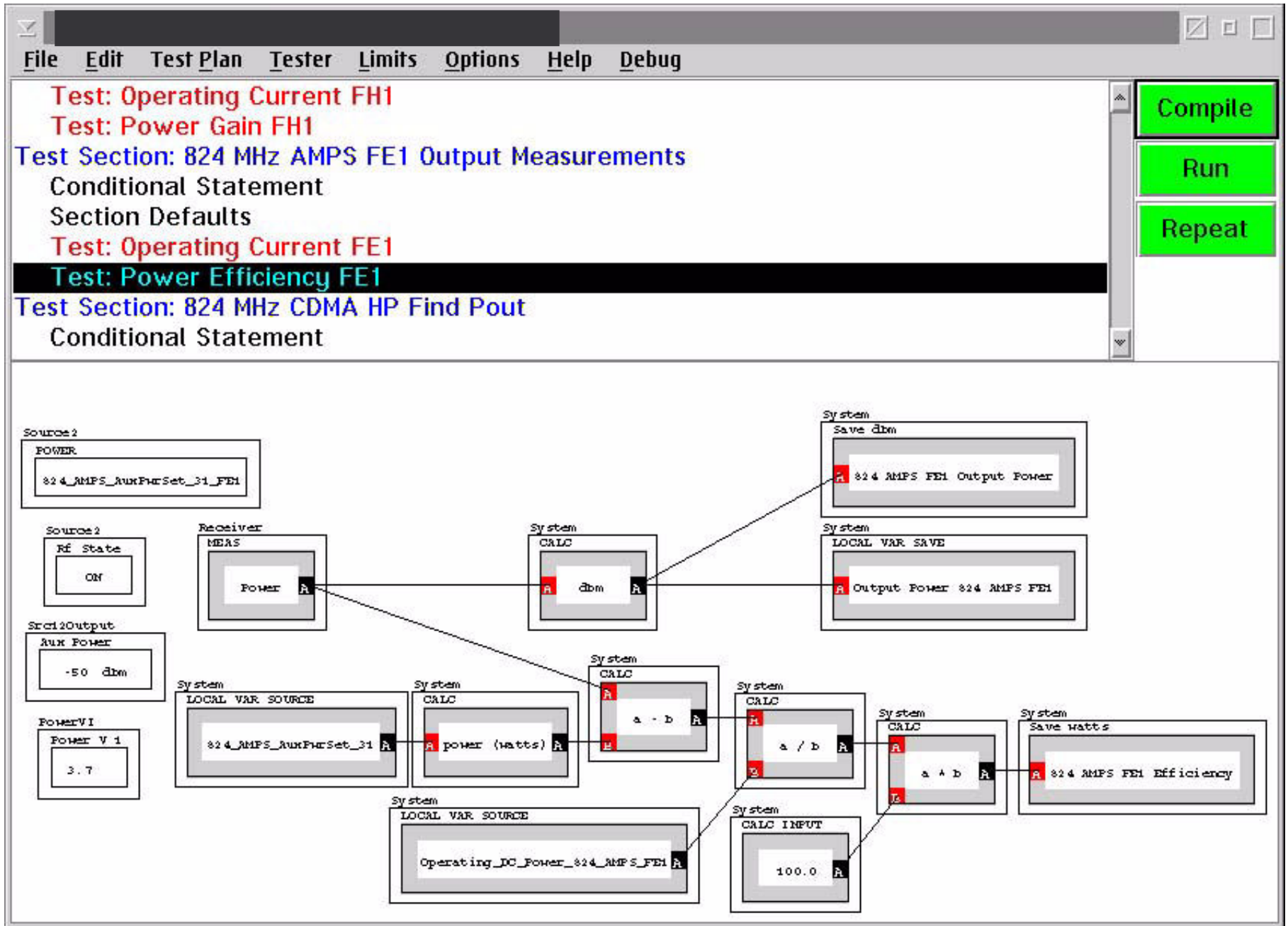


# Set Source 2 Input Level using Local Variable, DUT Pout = 31 dBm, Measure Icc





# Measure Pout and Calculated PAE for the DUT







# Measure Current using VI1 Imeasure BW set to Slow

File Edit Test Plan Tester Limits Options Help Debug

Test: CDMA HP Sweep Calc  
Test Section: 849 MHz CDMA Output Measurements HP  
Conditional Statement  
Section Defaults  
Test: Operating Current  
Test: Pin  
Test: Prefl\_RL  
Test: Channel Power  
Test Section: 849 MHz CDMA LP Find Pout

Compile  
Run  
Repeat

PowerVI  
IMEASURE BW  
slow

Src12Output  
AUX POWER  
849\_CDMA\_HP\_AuxPwrSet\_28

System  
Averages  
64

PowerVI  
MEAS  
Current A

CURRENT MEAS MAX  
1

IMEASURE  
v1

PowerVI  
INSTR STATE SOURCE  
PowerV1 A

System  
CALC INPUT  
1000.0 A

System  
CALC  
a + b A

System  
CALC  
a + b A

System  
Save Amps  
849 CDMA H Operating Icc A

System  
LOCAL VAR SAVE  
Operating\_DC\_Power\_849\_CDMA\_H A



# Measure Input Return Loss of a Modulated Signal

File Edit Test Plan Tester Limits Options Help Debug

Test: CDMA HP Sweep  
Test: CDMA HP Sweep Calc  
Test Section: 824 MHz CDMA Output Measurements HP  
Conditional Statement  
Section Defaults  
Test: Operating Current  
Test: Pin  
Test: P~~ref~~RL  
Test: Channel Power

Compile  
Run  
Repeat

Src12output  
AUX POWER  
824\_CDMA\_HP\_AuxPwrSet\_28

Testhead  
Parameter  
k1

Testhead  
Rec Attenuation  
0db

Receiver  
MEAS  
RMS Power A

System  
CALC  
dbm A

System  
LOCAL VAR SOURCE  
824\_CDMA\_H\_Pin A

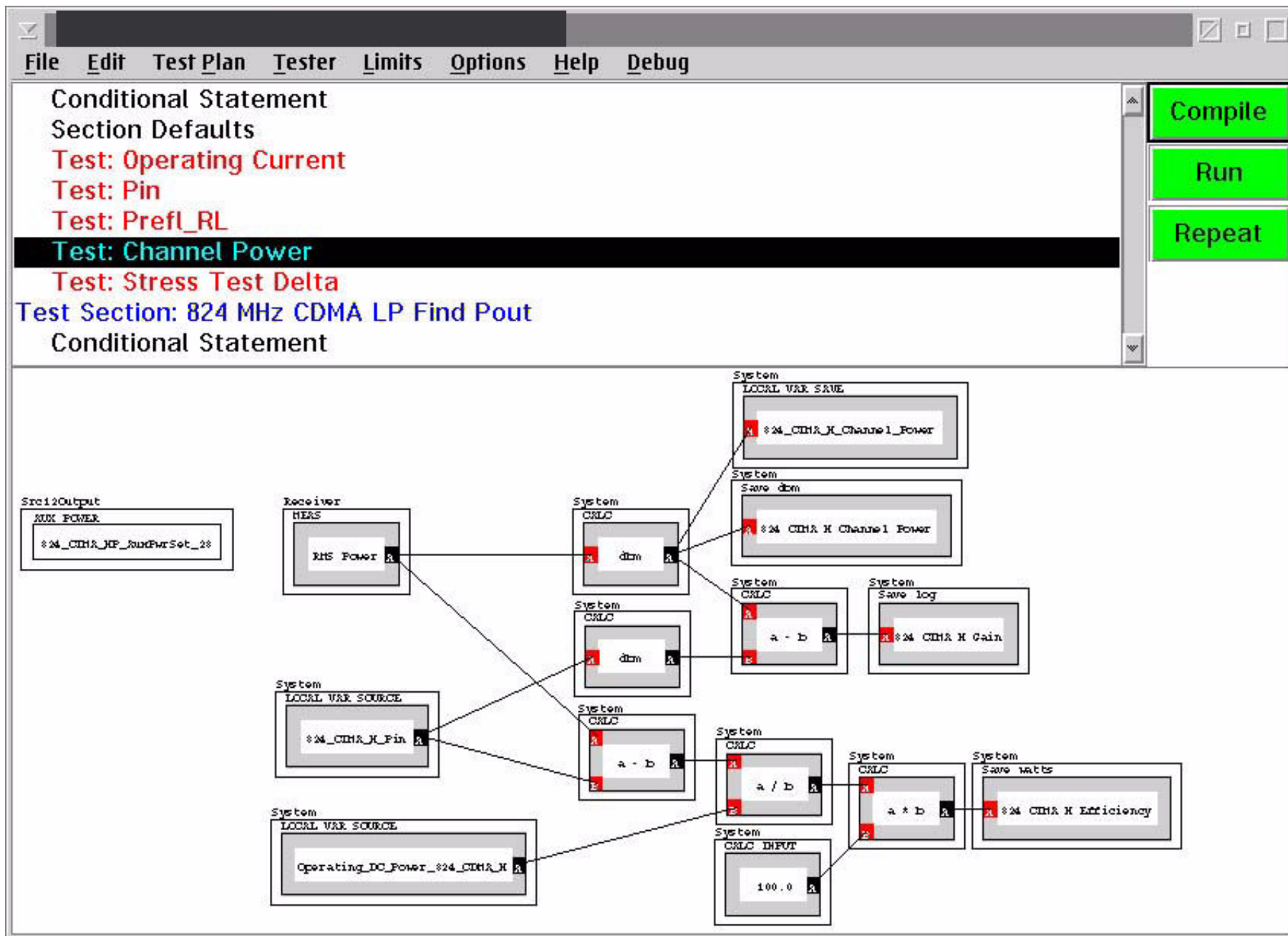
System  
CALC  
dbm A

System  
CALC  
a - b A

System  
Save log  
24 CDMA H Input Return Los



# Measure Pout, Calculate Gain & PAE of the DUT with an RF Modulated Signal applied





# Measure Current using DB 1 Voltage Parametric Capability

File Edit Test Plan Tester Limits Options Help Debug

Test Section: 824 MHz CDMA Output Measurements LP

Conditional Statement

Section Defaults

Test: Operating Current

Test: Ireg Low

Test: Imode Low

Test: Pin

Test: Prefl\_RL

Test: Channel Power

Compile

Run

Repeat

Sml2Output  
AUX POWER  
824\_CDMA\_LP\_AuxPwrSet\_16

StaticDigital  
Measure Mode  
Imeas

StaticDigital  
Measure V Force  
2.8

StaticDigital  
Measure Pin  
DB1

StaticDigital  
Db 1  
open

StaticDigital  
Current Meas Max  
0.002

StaticDigital  
Measure I Limit  
0.002

System  
MEAS  
Current A

System  
CALC  
a \* b A

System  
CALC INPUT  
1000.0 A

System  
Save Amps  
824 CDMA L Imode Low



# Measure ACPR using Receiver Frequency Offset Button

File Edit Test Plan Tester Limits Options Help Debug

Test Section: 824 MHz CDMA ACPr Measurements HP/LP, added Rec Freq offset

Conditional Statement

Section Defaults

**Test: Alternate Low LP**

Test: Alternate Low HP

Test: Adjacent Low HP

Test: Adjacent Low LP

Test: Adjacent High LP

Test: Adjacent High HP

Compile

Run

Repeat



# Measure Second Harmonic

File Edit Test Plan Tester Limits Options Help Debug

Test: Adjacent High HP  
Test: Alternate High HP  
Test: Alternate High LP  
Test Section: 824 MHz AMPS Harmonic Measurements  
Conditional Statement  
Section Defaults  
**Test: 2nd Harmonic FE1**  
Test: 3rd Harmonic FE1  
Test Section: 849 MHz CDMA HP Find Pout

Compile  
Run  
Repeat

PowerVI  
Power V 1  
3.7

Receiver  
FREQUENCY  
MASTER  
Source2  
CONFIG  
Frequency  
SCALE  
2  
OFFSET  
0

Source2  
Rf State  
ON  
Sml2Output  
Aux Power  
-50 dbm  
Sml2Output  
AUX POWER  
824\_AMPS\_AuxPwrSet\_31

System  
LOCAL VAR SOURCE  
Output Power 824 AMPS FE1

Receiver  
MEAS  
Power

System  
CALC  
dbm

System  
CALC  
a - b

System  
Save log  
824 AMPS 2nd Harmonic



# Measure Third Harmonic

File Edit Test Plan Tester Limits Options Help Debug

Test: Adjacent High HP  
Test: Alternate High HP  
Test: Alternate High LP  
Test Section: 824 MHz AMPS Harmonic Measurements  
Conditional Statement  
Section Defaults  
Test: 2nd Harmonic FE1  
**Test: 3rd Harmonic FE1**  
Test Section: 849 MHz CDMA HP Find Pout

Compile  
Run  
Repeat

PowerVI  
Power V 1  
3.7

Receiver  
FREQUENCY  
MASTER  
Source2  
CONFIG  
Frequency  
**SCALE**  
3  
OFFSET  
0

Source2  
Rf State  
ON  
Src12Output  
Aux Power  
-50 dbm  
Src12Output  
AUX POWER  
824\_AMPS\_AuxPwrSet\_31

System  
LOCAL VAR SOURCE  
Output Power 824 AMPS FE1

Receiver  
MEAS  
Power

System  
CALC  
a - b

System  
CALC  
dbm

System  
Save log  
824 AMPS 3rd Harmonic



# Sweep Power to Find Gain Slope

## Use Lock Step to Control Receiver Attenuation

File Edit Test Plan Tester Limits Options Help Debug

Test Section: Gain Slope GSM (Unoptimized)  
Conditional Statement  
Section Defaults  
**Test: Gain Slope L**  
Test: Gain Slope H  
Test: Calculation Low Power Log  
Test: Calculation High Power Log  
Test: Calculation High Power Linear  
Test Section: GSM Tests (Unoptimized)

Compile  
Run  
Repeat

LOCK STEP CONFIG

PowerVI	Testhead
Power V 3 1.08	Rec Attenuation 20db
Power V 3 1.09	Rec Attenuation 20db
Power V 3 1.1	Rec Attenuation 30db
Power V 3 1.12	Rec Attenuation 30db
Power V 3 1.14	Rec Attenuation 30db

Receiver  
If Gain  
44

PRE MEAS  
PowerVI: Power V 3 (A)  
System: Sequence Delay (0)

POST MEAS  
PowerVI: Power V 3 (0)

PowerVI: INSTR STATE SOURCE (PowerV3) → System: LOCAL VAR SAVE (V\_Gn\_Slp\_GSM)

Receiver: MEAS (Power) → System: CALC (dbm) → System: LOCAL VAR SAVE (P\_db\_Gn\_Slp\_GSM)

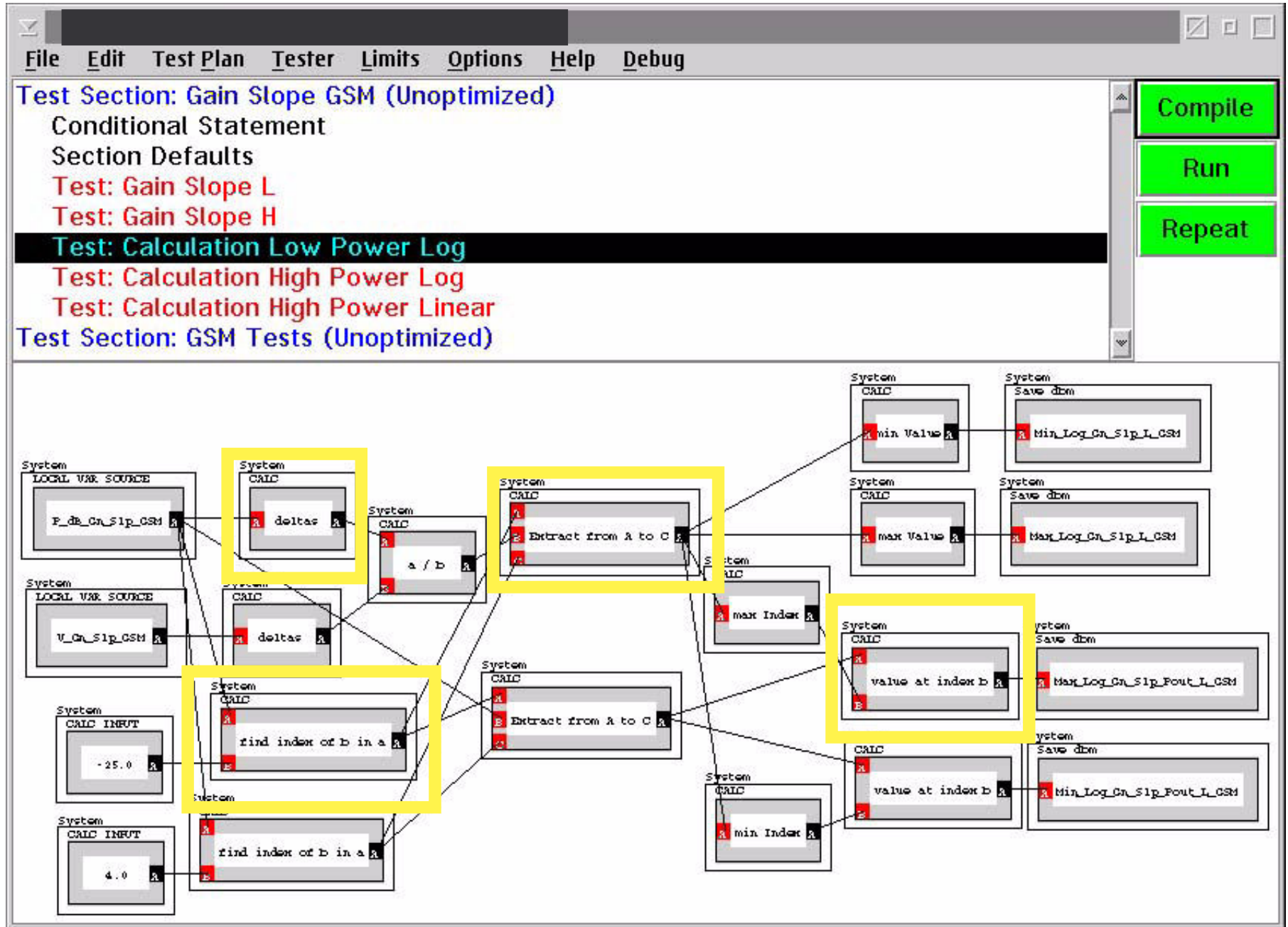
System: CALC (voltage) → System: CALC (a \* b) → System: LOCAL VAR SAVE (P\_VGn\_Slp\_GSM)

System: CALC INPUT (1.414)





# Calc Gain Slope using Deltas, Extract, Find Index & Value at Index





# Set Source 1 Mode to Noise: Isolates Source 1 from DUT Measure Pulsed Idle Current

The screenshot shows a software interface with a menu bar (File, Edit, Test Plan, Tester, Limits, Options, Help, Debug) and a list of tests on the left. The test 'Test: Idle current' is selected and highlighted in black. On the right, there are three green buttons: 'Compile', 'Run', and 'Repeat'.

The main area contains a block diagram with the following components:

- Source1**: A block containing a 'Frequency' field with the value '915 Mhz'.
- PRE MEAS**: A block containing a 'PowerVI' sub-block with a 'Power V 3' field set to '1.7'.
- POST MEAS**: A block containing a 'PowerVI' sub-block with a 'Power V 3' field set to '0'.
- Testhead**: A block containing a 'Source 1 Mode' field set to 'noise'. This block is highlighted with a yellow border.
- PowerVI MEAS**: A block containing a 'Current' field with a unit symbol 'A'.
- CURRENT MEAS MAX**: A block containing a field with the value '1'.
- IMEASURE**: A block containing a field with the value 'v1'.
- System CALC**: A block containing a calculation field 'a + b' with unit symbols 'A' on both sides.
- System CALC INPUT**: A block containing a field with the value '1000.0' and a unit symbol 'A'.
- System Save Amps**: A block containing a field 'Idle\_Current\_GSM' with a unit symbol 'A'.

Connections in the diagram: The 'Current' field of the 'PowerVI MEAS' block is connected to the 'a' input of the 'System CALC' block. The 'System CALC INPUT' block is connected to the 'b' input of the 'System CALC' block. The output of the 'System CALC' block is connected to the 'Idle\_Current\_GSM' field of the 'System Save Amps' block.

**NOTE**



# Measure Vpc Pin Leakage Current using DB Line

The screenshot shows a test plan editor window with the following menu: File, Edit, Test Plan, Tester, Limits, Options, Help, Debug.

Test: Output Pwr L  
Test: Output Pwr H  
Test: Efficiency  
Test: Idle current  
**Test: Vpc Leakage**  
Test: Power Dn Current

Test Section: Gain Slope DCS (Unoptimized)  
Conditional Statement  
Section Defaults

Buttons: Compile, Run, Repeat

Block Diagram:

- PowerVI: Power V 1 (5.3)
- Source1: Frequency (915 Mhz)
- PowerVI: Power I 3 (0)
- System: Averages (1)
- PowerVI: V 3 Output (OFF)
- Testhead: Source 1 Mode (noise)
- StaticDigital: Measure Mode (I meas)
- StaticDigital: Measure V Force (0.5)
- StaticDigital: Measure Pin (DB3)
- StaticDigital: Current Meas Max (20 u)
- StaticDigital: Measure I Limit (20 u)
- StaticDigital: MEAS (Current A)
- System: CALC (a + b A)
- System: CALC INPUT (1000000.0 A)
- System: Save Amps (Vpc Leakage\_GSM\_uA)

NOTE



# Measure Power Down Current Using VI to set Voltage Level & DB to Measure Current

**File Edit Test Plan Tester Limits Options Help Debug**

Test: Output Pwr L  
Test: Output Pwr H  
Test: Efficiency  
Test: Idle current  
Test: Vpc Leakage  
**Test: Power Dn Current**

Test Section: Gain Slope DCS (Unoptimized)  
Conditional Statement  
Section Defaults

**Compile**  
**Run**  
**Repeat**

**Pre Meas**

- StaticDigital: Measure V Force (5.3)
- StaticDigital: Measure Pin (DB1)
- PowerVI: V 1 Output (OFF)
- System: Sequence Delay (100)

**Post Meas**

- PowerVI: V 1 Output (ON)
- StaticDigital: Measure Pin (None)
- StaticDigital: Measure V Force (0)

**Block Diagram:**

- StaticDigital: MEAS (Current A)
- System: CALC (a + b A)
- System: Save Amps (Power\_Dn\_Current\_GSM\_uA)
- System: CALC INPUT (1.0e9 A)

**Other Parameters:**

- PowerVI: Power V 1 (5.3)
- PowerVI: Power I 1 (0)
- PowerVI: V 3 Output (OFF)
- PowerVI: Power I 3 (0)
- Source1: Frequency (915 Mhz)
- Testhead: Source 1 Mode (noise)
- System: Averages (16)
- StaticDigital: Measure Mode (I meas)
- StaticDigital: DB 3 (off)
- StaticDigital: Measure I Limit (200 u)
- StaticDigital: Current Meas Max (200 u)

NOTE