Synthetic DSP Approach for Novel FPGA-Based Measurement of Error Vector Magnitude

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Abstract

A new implementation of EVM measurement has been developed in a production test environment using an FPGA-based DSP processor within an ATE test solution. The focus of interest is in identifying key areas of the DSP that affect measurement quality and optimizing their execution on an FPGA to increase measurement accuracy, precision, repeatability, and reduce test time. This approach defines a real-time processing methodology for signal demodulation and EVM calculation as opposed to traditional PC-based post processing and offline computation of EVM. The analysis of the DSP elements and their corresponding error artifacts are presented in a standard approach to EVM measurement. The experimental results of the digital demodulation system and EVM measurement in MATLAB/Simulink are compared against a bench-top Rohde&Schwarz complex signal generator and vector signal analyzer to qualify the results.

Index Terms— Digital Signal Processing (DSP), Vector Signal Analyzer (VSA), Error Vector Magnitude (EVM), Design For Test (DFT), Device Under Test (DUT), Field Programmable Gate Arrays (FPGA), Automated Test Equipment (ATE), Finite Impulse Response (FIR), Radio Frequency Integrated Circuits (RFIC).

1. Introduction

With the advent of advanced silicon processes, the complexity of telecommunication RF ICs and system-on-chip transceiver architectures continue to increase. The integration of digital, analog, and RF on a single die offers more efficient and tightly integrated systems with higher performance and lower manufacturing costs. However, this design approach complicates test and debugging by making it prohibitively expensive in execution. On the IC side, silicon area is sacrificed in DFT schemes in addition to the added complications of design integration inherent with embedded test. Within production test, considerable efforts to implement design for test schemes and test plan optimization require substantial development effort [1] and [2]. With more integrated RFICs, parallel and sequential subsystem test points become laborious, test plans become increasingly complex, and the results do not definitively qualify the overall operation of the DUT.

EVM has become the predominant choice to fill this test space, offering a critical figure of merit that encapsulates all of the linear and non-linear errors of a transceiver system by stimulating and measuring the circuit/system the same as would be under normal operating conditions [3]. The current problem is that functional EVM requires a significant amount of captured data and DSP to achieve valid results. The difficult task has been determining a way to speed up the test time in an ATE environment without sacrificing accuracy. The test can become cost prohibitive because of prolonged test times associated with the large data sets, and the test plan is difficult to adapt to new and changing standards due to ATE equipment's specialized hardware. Optimizations to the test setup and processing techniques using synthetic instrument approaches have begun to show promise [4], [5] and [6]. In [7] and [8], reduced test time and measurement reliability improvements have been demonstrated by identifying "worst-case" input scenarios, reducing the input test cases, and expanding the "pass-fail criteria" to improve yield loss. In [9], [10], and [11], techniques to extract EVM from single or combinations of simpler communication test measurements show a means of bypassing the difficulties in conducting an EVM test on a more complex DUT. Research in [12], [13], and [14] employ the use of algorithms developed from models of simple test components to extract EVM from various other test metrics. However, these strategies require highly accurate behavior models and complex algorithms to account for the test responses and translate the results into EVM. Even with intensive data processing, the resulting EVM measurement has varying degrees of error that can range from approximately 0.5% to 12%, depending on the accuracy and complexity of the DUT model.

The proposed solution in this discussion is an FPGA-based co-processor that functions as a medium between the ATE's hardware infrastructure and processing core to provide additional computational capacity, flexibility, and speed. FPGA's provide a number of advantages: powerful development/synthesis tools, dedicated DSP capabilities, and the infrastructure to interface with high speed I/O. These provide the capability to compute EVM while reducing or eliminating the overhead associated with passing large packets of data from the data capture hardware to the PC within the ATE, drastically decreasing the test time. This approach also eases execution by eliminating the need for model-based

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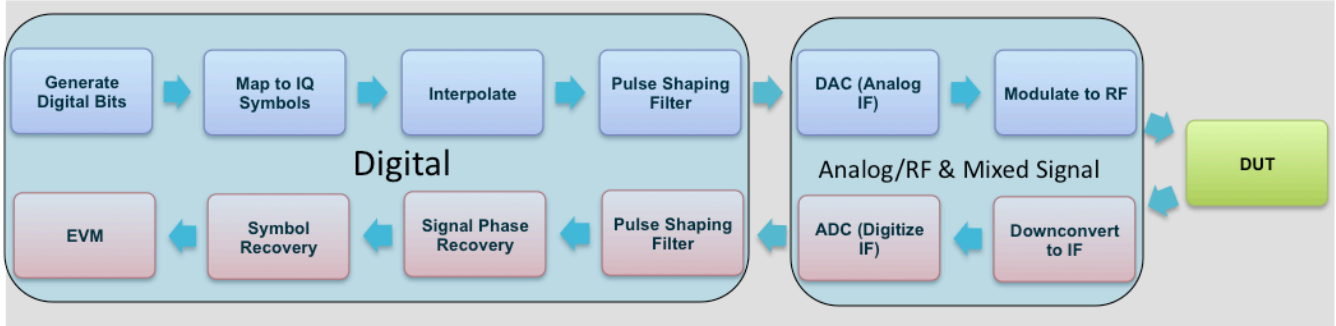

Fig 1: Generic Flow Diagram for Measuring EVM from a DUT: Modulated Signal Generation (Blue/top path), Signal Demodulation and EVM (Red/Bottom Path). Each flow path is broken down into its' corresponding digital and RF/analog paths

analysis of the DUT, allowing for complex and highly integrated systems to be tested without any a priori data. The reconfigurable DSP fabric of the FPGA provide a framework that allows for a flexible platform that can support multiple applications and emerging standards with reduced development cycles.

The following discussion focuses on the development of an FPGA DSP processor to compute EVM for M-ary QAM signals used in WLAN protocols. The Background section introduces the overall test structure for the computation of EVM, basic de/modulation concepts, and corresponding subsystems involved in the measurement. The Method and Materials section discusses the measurement implementation on the FPGA: DSP blocks/subsystems for computing EVM, overall footprint of the design, pathways for supporting multiple applications, potential computation time improvements, and sources of error inherent in this approach. The Results and Analysis section provides quantitative results of the error sources, comparison to standard bench top equipment, and strategies for mitigation.

2. Background

EVM directly links the digital and analog parts within a radio by quantifying the signal's modulation accuracy [15], [16]. In order to transmit data, the information is translated to its analog counterpart by means of a modulation scheme; an example of 16-QAM is depicted in Fig 2a. During the various stages of the modulation and demodulation, digital, analog, and RF impairments manifest themselves in the symbol constellation as deviations from the ideal symbol points. EVM is simply the vector subtraction in the IQ plane of the measured symbol from the ideal symbol as depicted in Fig 2b. The analysis of the individual error vectors or instantaneous EVM gives feedback on individual test signal cases through the transceiver system. These can fluctuate significantly depending on the DUT and in non-ideal cases, by the tester system's DSP. To alleviate these fluctuations and provide consistency in the measurement, EVM is typically an averaged value over a set of symbols, see Eqn 1.

$$AverageEVM_{\%RMS} = \sum_{n=1}^{N} \frac{\sqrt{[I(n)_{Meas} - I(n)_{Ref}]^2 + [Q(n)_{Meas} - Q(n)_{Ref}]^2}}{[I(n)_{Meas} + Q(n)_{Meas}]^2} \times \frac{1}{N} \times 100\% \quad (1)$$

The process of measuring EVM has three main components: generate the input test signals, capture the modulated output signal, and process the data. The test setup can vary depending on the type and complexity of the DUT, but Fig 1 demonstrates the general signal flow of the modulation, demodulation, and measurement subsystems. Focusing on the receiver side, once the signal from the DUT is digitized, the task of deconstructing the data down to the necessary IQ symbols to compute EVM relies on intensive signal processing: pulse shaping filtering, phase recovery, and symbol timing recovery before evaluating the recovered symbols to measure EVM. Working backwards through the measurement receiver, the phase recovery system is responsible for correcting phase rotations of the IQ symbols to the correct orientation. The symbol timing recovery system differentiates the IQ symbols at their corresponding coding rate. The symbol and phase recovery techniques are data driven mechanisms, meaning their accuracy is directly related to the quality of the data that is input. Therefore errors generated by the filter inherently affect the downstream processes by corrupting the symbols that are recovered. Since the recovered symbols drive the heart of the mathematics behind the EVM measurement, the source of the measurement's precision relies heavily on the design, synthesis, and implementation of the filter and symbol timing recovery.

Raised cosine pulse-shaping filters are a type of finite impulse response filter that provide band limiting of the signal used in various protocols, specifically WLAN in this case. They are used to improve bandwidth channel efficiency while ensuring no inter-symbol interference (ISI) by means of a roll-off variable (alpha). Eqn 2 provides the mathematical expression of the frequency response and Eqns 3 and 4 show the corresponding time domain expression. In Fig 3, effects of varying the rolloff can be seen in the frequency response across the range of alpha: 0 (no excess bandwidth) to 1 (transition bandwidth=pass band bandwidth).

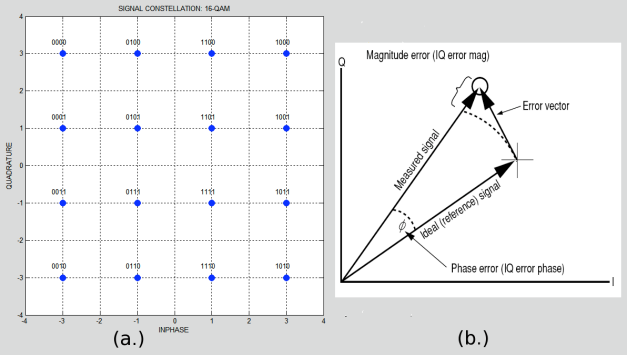

Fig. 2: (a.) Example of a 16-QAM constellation and bit coding; (b.) vector representation of EVM and related components

$$H(f)=\begin{cases} T, |f| \le \dfrac{1-\alpha}{2T} \\ \dfrac{T}{2}\left[1+\cos\left(\dfrac{\pi T}{\alpha}\left[|f|-\dfrac{1-\alpha}{2T}\right]\right)\right], \dfrac{1-\alpha}{2T} \prec |f| \le \dfrac{1+\alpha}{2T} \\ 0, otherwise \end{cases} \quad (2)$$

$$0 \le \alpha \le 1$$

$$h(t)=\sin c\left(\frac{t}{T}\right)\frac{\cos(\pi\alpha t)}{1-\dfrac{4\alpha^2 t^2}{T^2}} \quad (3)$$

where

$$\sin c(x)=\frac{\sin(\pi x)}{\pi x}$$

$$\alpha = 2T\Delta f = \frac{\Delta f}{R_S/2} \quad (4)$$

where

$$R_S = \frac{1}{T}$$

In practice, raised cosine filters are split between the transmitter and receiver by implementing a square-root raised cosine filter in each. This creates a pair of matched filters that ease design complexity and promote consistency by partitioning the design between the two paths. When implementing half of the filter in both the paths, it becomes of high importance to insure the roll-off characteristics remain the same. Any discrepancies between the two, result in a non-ideal representation of the overall filter. This mismatch then translates directly into error of the recovered signal that propagates through the demodulation process and appears as additive error measured in EVM.

Being in the front-end of the digital demodulation process in the FPGA places special importance on the design constraints of the filter. Errors manifested here proliferate through the demodulation chain and contribute to the overall precision of the EVM measurement. Specifically there are three distinct cases of high importance when implementing the design on an FPGA:

- Errors caused by mismatch of the roll-off factor between the DUT's filter and the EVM tester's filter
- Filter approximation error stemming from limited filter order in the synthesis process
- Quantization errors associated with fixed-point representation of the filter coefficients

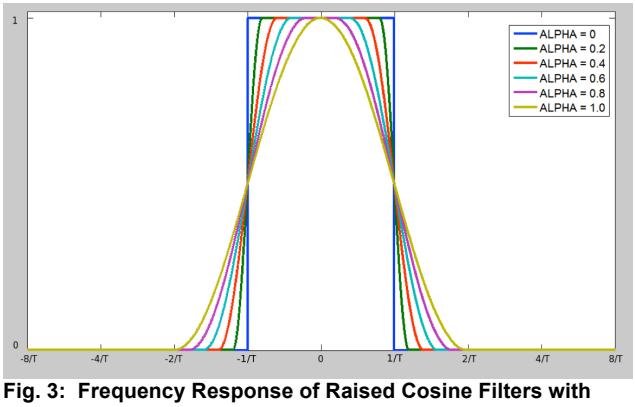

Fig. 3: Frequency Response of Raised Cosine Filters with varying roll-off (alpha). Larger alpha relates to relaxed transition band roll off

3. Experimental Methods & Materials

As the first step in the development of an FPGA based EVM measurement the focus of interest was the analysis of systemic error phenomena generated by the DSP components. This would establish system and subsystem design criteria for an implementation in a currently available FPGA to define measurement accuracy and precision limitations. The target platform is a low cost, low power Altera Cyclone III with 8Mbits of embedded memory, 396 multipliers, and 200K logic elements. The targeted DSP implementation was the use of less than 50% of the available logic resources on the FPGA for filtering, symbol timing recovery, and EVM. This was to allow for future test expansion in a synthetic instrument capacity, as well as to reserve resources that could be utilized for processing speed enhancements such as parallelization and data pipelining. Since the pulse-shaping filter plays a critical role in the overall accuracy of the EVM measurement, this is the focal point of error analysis.

Taking into consideration the physical limitations of the amount of DSP resources available in the FPGA, the design strategy was to minimize errors in the EVM calculation while seeking a balance of reduced design footprint and maximum computation speed. The mechanisms in the filter design that translate directly to these performance metrics are: filter order, filter mismatch, and fixed-point approximation. The test signals for all cases were a QPSK signal with 8x oversampling to mimic a conventional digitized data stream from an ADC. QPSK signals were chosen due to their high sensitivity to error in the EVM measurement [19] and their use as a subset of M-ary QAM in WLAN protocols. The findings

for this modulation can be translated to higher order QAM as the filter type, symbol recovery, and EVM computation use the same underlying DSP structure and functions.

3.1 Filter Mismatch Experiment Setup

To isolate and characterize mismatch behavior between the filters in terms of EVM, a worst-case scenario model was developed. The test system was designed using Simulink, emulating the digital portion of the architecture demonstrated in Fig 1: The output signal from the pulse-shaping filter in the transmitter is fed directly into the pulse-shaping filter in the receive path, simulating an ideal digital transceiver path using root-raised cosine filters. The test signal was a 1MHz QPSK modulated signals with a roll-off factor (alpha) of 0.1, driving a bank of root-raised cosine filters in the receiver portion with alphas spanning the range of values from 0.1 – 1. Squaring-timing recovery was used for symbol recovery, and both instantaneous and averaged EVM was calculated on the recovered symbols.

The same experiment was conducted using a Rohde&Schwarz(R&S) SMIQ complex signal generator and FSIQ vector signal analyzer, and the results were compared. The signal generator's alpha was swept from 0-1 while the signal analyzer's alpha was fixed at 0.1 to recreate the test setup in Simulink. An arbitrary 1MHz QPSK signal with a 2.4GHz RF carrier was generated using the same flow as shown in Fig 1 by the SMIQ.

3.2 Filter Order Synthesis Setup

Another source of unavoidable error in the filter design is caused by limited filter order. For any digital filter design, the number of coefficients or taps is finite, thus the amount of taps used directly correlate with the precision of the resulting filter response. Errors introduced by this limitation have a pronounced effect on the recovered symbols and resulting EVM measurement. This filter order is a vital design parameter when implemented on the FPGA because a trade-off between EVM precision, and DSP resources have to be taken into consideration. This test setup is identical to the filter mismatch experiment, with the difference of replacing alpha error with filter order as the independent variable. Since this type of error is exacerbated by sharper roll-off characteristics in the filter synthesis, the worst-case scenario of a 0.1 alpha was analyzed. The range of filter size in the experiment extended from an extremely simple design of 16 taps to 512 taps. This provided a broad range of practical design choices that span from a small design footprint of ~1-2% of the total DSP resources to a rigorous design encompassing ~25% of the total usable DSP on the FPGA.

3.3 Fixed-point Approximation Setup

Sharing similarities with the test setups for filter mismatch and filter order, the fixed-point analysis was also conducted with a bank of matched filters on the tester's receiver chain, and the filter's number of coefficients ranges from 10 taps to 500 taps. The filter synthesis process includes the additional step that once all of the coefficients for a specified filter order are specified with floating-point precision, they are then approximated to fixed-point values of 8-bit and 16-bit representations. These two bit types were selected for their ubiquitous use for bus size of various digital components to represent practical data bit widths that would be expected from an ATE data capture module. As the intent is to position the FPGA between this module and the PC, this represents an ideal case scenario to examine. By varying the filter size, the effects of fixed-point approximation can be related to the effects seen with filter order. This test scenario mimics an implementation that would be rendered on an FPGA to again seek an optimum solution for the filter design.

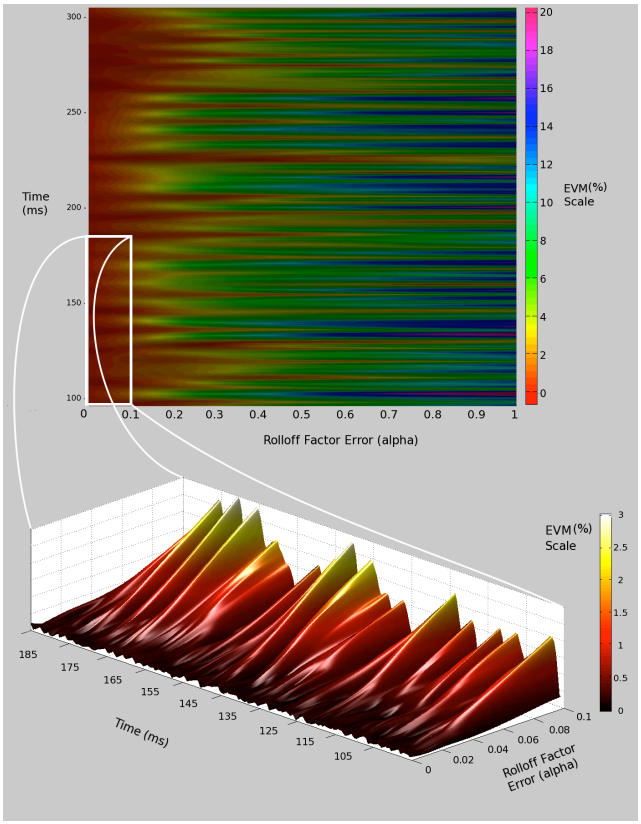

Fig. 4: (Upper Graph) Chromatogram showing variation in instantaneous EVM over time/recovered symbols (y-axis) versus mismatch error (x-axis); (Lower Graph) Zoomed-view of variations in EVM across 0 -0.1 Roll off Error

4. Results & Analysis

4.1 Filter Mismatch

The measured instantaneous EVM provides a means for analyzing individual error vector behavior, as seen in the top portion of Fig 4. As the mismatch is increased, the variation of instantaneous EVM values also increases. The combination of the mismatched pair of square-root raised cosine filters creates a filter response

that no longer satisfies the criteria for no ISI. The byproduct of this filter response is distortion error of the output signal that is input to the symbol recovery stage. Since the symbol timing recovery system is a data driven-mechanism, the quality of the recovered symbols is determined by the quality of the input signal. Since the original QPSK signal is pseudo-random, the resulting ISI is also random, and the error behavior of filter mismatch in the EVM measurement is essentially indistinguishable from noise.

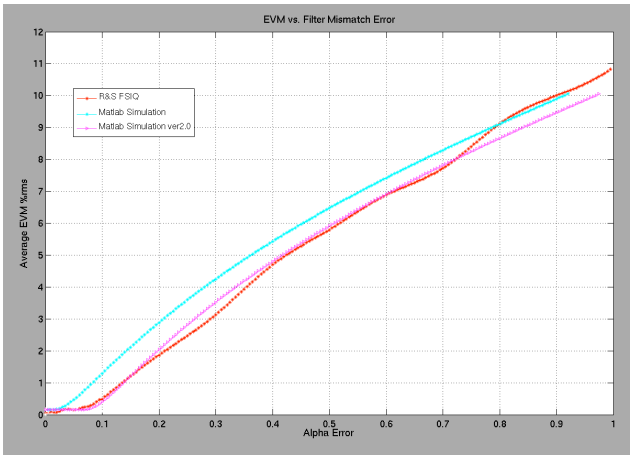

Fig. 5: Comparison of Measured Average EVM from a R&S FSIQ (red) as a function of filter mismatch to simulation models (magenta; cyan) developed in MATLAB/Simulink. Version 2 plot is an offset of the original simulation used as a comparison reference

At the maximum alpha error, instantaneous EVM can span a range of 0.5% - 20%. In the bottom graph of Fig 4 where the mismatch is small, the overall instantaneous EVM is reduced and more stable, residing in a region of 0.05% - 3%. It's observable that even though EVM has a much lower nominal value, it still maintains the "random" behavior that is seen on a larger alpha error scale, except with reduced excursions. This region represents typical residual mismatch seen between differing filter building tools when synthesizing each root-raised filter to the same alpha. It is important to note that even in regions of less than 0.01 mismatch error, small perturbations in EVM are on the order of 0.001% - 0.1%. This demonstrates limitations in instantaneous EVM precision that are driven by other mechanisms in the filter implementation that will be discussed in the following sections.

The results of the average EVM experiment are compared in Fig 5 with two iterations of the Simulink models and data captured from the Rohde&Schwarz VSA. The difference between the first and second iteration of the Simulink models is simply an alpha offset to provide a reference point for better comparison. The difference between the original simulation data and measured data can be attributed to design differences in the symbol timing recovery and channel equalization techniques used in the FSIQ's DSP but not adequately represented in the Simulink model. However, offset aside, there is a high correlation in the overall trend of the data between the modeled and measured data. This remains consistent across the entire span of possible alpha and provides a reasonable basis of the efficacy of the Simulink model approach in characterizing the relationship between EVM and filter mismatch. Table A in the Appendix provides a chart quantifying the results presented in the graph.

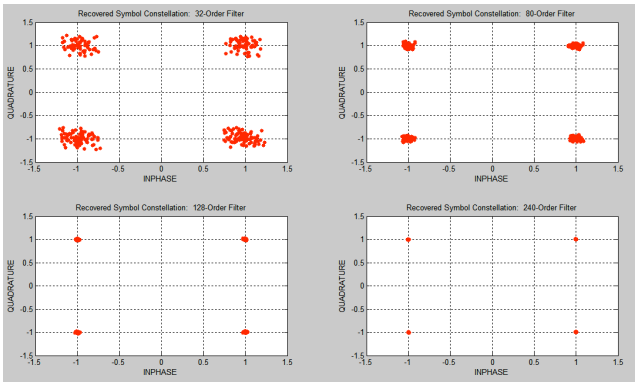

Fig. 6: Recovered QPSK Symbol Constellations from Different Pulse-Shaping Filter Orders: 32-Order (top left); 80-Order (top right); 128-Order (bottom left); 240-Order (bottom right)

4.2 Filter Order Discussion

In an effort to quantify the design tradeoff of EVM precision and FPGA resources used for filter synthesis, the results in Fig 6 represent the recovered QPSK symbols with various filter orders used in the receiver path. As the filter order is increased, the resulting symbol points' spread of +/- 0.25 reduces to a tighter grouping of +/- 0.01 around the ideal IQ symbol points of {I: +/-1, Q: +/-1}. As was the case for filter mismatch, this type of error is seen as random dispersion of the symbol points in the I/Q constellation. As shown in Fig 7, the corresponding EVM error behavior was modeled across the range of filter orders from 16 to 500 for three matched filter designs with alpha values of 0.1, 0.4, and 0.7. The EVM error demonstrates a dependence on the roll-off characteristics selected. This error is more pronounced in the lower alpha cases for smaller orders due to the more severe roll-off requirements between the pass band and stop band in the frequency domain. In order to approximate this transition, the filter exhibits Gibbs phenomenon in the regions of the pass and stop band adjacent to the transition. As the filter order is increased, the ripples' effect on the overall filter response in this region is diminished. The resulting filter approximation error translates into a wide range of EVM error: 19%rms +/-8% with a filter order of 16 to 0.1%rms +/- 0.01% with a filter order of 512. As alpha is relaxed to 0.4 and 0.7, this overall effect on EVM is diminished, reducing the corresponding 16-order filter EVM error to 10.2%rms+/-4.5% for an alpha of 0.4 and 4.1%rms+/-2.2% for an alpha of 0.7. The curves share asymptotic behavior as filter order is increased, and an optimum filter order of greater

than 140 was found to produce a minimum EVM error. From a design perspective, this error phenomenon depended on the interaction of filter order and filter design parameters, specifically the relationship between alpha, the modulation rate, and sample rate to optimize the EVM accuracy. As such, different combinations of these design parameters will yield a different optimum order.

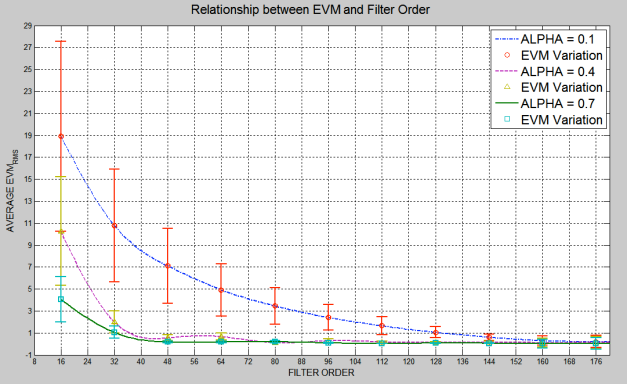

Fig. 7: Relationship between EVM Error and Filter Order for roll-off values of: 0.1, 0.4, and 0.7

4.3 Fixed-Point Errors

Fixed-point approximation errors are most easily viewed and interpreted in the frequency domain. In Fig 8, a comparison of the floating-point precision frequency response of a pulse-shaping filter to that of its corresponding fixed-point approximation is shown. The largest deviations from the ideal floating-point filter response occur mostly in the stop band where the resulting signal components are of nominal interest. In terms of the impulse response, this refers to the regions in the outlying sides lobes, where the coefficient values asymptotically approach zero according to the sinc function. As the filter order is increased, the number of coefficient values with precision error will increase, but these added contributors

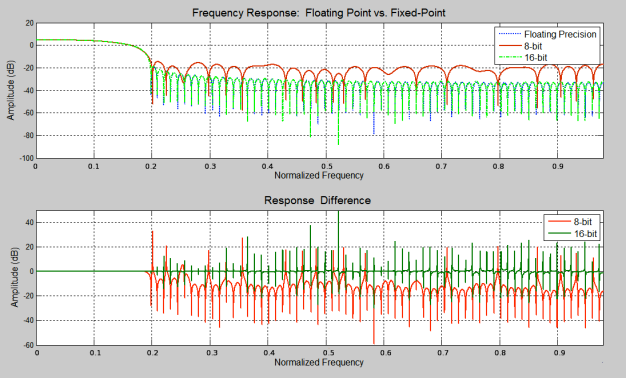

Fig. 8: 8-bit and 16-bit Fixed-Point vs. Floating-point Precision Frequency Response (top) and corresponding differences (bottom)

are located mainly in the stop band region where the distortion effects are minimal. Accordingly, errors generated by fixed-point approximation of 8 and 16bit word lengths account for very small contributions to the overall EVM error. Table B in the Appendix further quantifies this point, showing worst-case EVM errors stemming from this process are relegated to approximately 0.45% in the worst case, and for the 16-bit case, well below 0.001% EVM error.

5. Conclusion

The experimental findings identified the pulse-shaping filter as a critical DSP component that ultimately plays a direct role in defining the precision of recovered symbols and the EVM measurement. Digital artifacts and errors generated by filter roll-off mismatch between DUT and tester, filter synthesis errors stemming from the number of coefficients used in the filter implementation, and quantization error from fixed-point coefficient values demonstrated various types of filter mismatch. It was observed that these types of error were virtually indistinguishable from random noise. A MATLAB simulation model was developed to establish a heuristic relationship between these precision limiting factors and the corresponding EVM inaccuracy. These types of signal degradation were recreated in bench-top hardware using a Rohde&Schwarz modulated signal generator and vector signal analyzer, showing a difference in EVM results between model and hardware of less than 0.5%. Subsequent tests relating EVM accuracy to filter order synthesis and fixed-point quantization yielded worst-case EVM errors of 19% and 0.45% respectively. From the 8x-oversampled test case, it was found that filter orders greater than 144, achieved EVM precision as high as +/-0.5% for a QPSK modulation scheme regardless of roll-off characteristics. The process demonstrated that in practice, the overall filter design could be optimized and implemented in an FPGA architecture with little more than 150 coefficient taps using 16-bit precision, and yielding EVM measurement's accuracy of +/-0.5%. This greatly improves the repeatability of the measurement while providing a clear and direct path for utilizing an FPGA's high performance DSP to reduce test time.

Design considerations and the developed DSP MATLAB elements could be implemented in a Cyclone III FPGA with a projected footprint of approximately 10% of the total logic resources for the filter realization, 23% for the symbol timing recovery, and 5% for the EVM measurement. With an overall architecture of roughly 40% of the total resources, there is considerable room for future test modules to support synthetic instrument or software-defined radio capabilities. Initial estimations of computation time within the FPGA for a 1MHz M-ary QAM signal with 8x oversampling are as follows: Filter Delay – 150us; Symbol Timing Recovery – 260us, EVM measurement 80us. This provides high flexibility and a low-test time that translates to lower test cost and improved time-to-market in the highly competitive IC industry.

6. Conclusions

With highly accurate models of the error sources in the front-end of the digital demodulation system and a means to minimize it's design footprint, further development of the symbol and phase timing recovery systems will be conducted. With the necessary demodulation and EVM measurement subsystems in place, a test of the implementation will be conducted on captured data to compare the computation speed performance of the proposed system. The results of the measurement precision and computation time between the FPGA platform, MATLAB simulations, and bench top equipment will be compared. The final step would be a real-time measurement of EVM on an RFIC for one or multiple application standards in an ATE environment. The computation speed and accuracy performance will be compared against the developed models to determine test times for RFIC's using various standards such as Bluetooth, WLAN, and WiMax.

7. Appendix

A.) **Comparison of Average EVM and Filter Mismatch of Simulation vs. Rhode&Schwarz FSIQ**

Alpha Mismatch	Simulink Ver1 / Ver2 EVM [% rms]	R&S EVM [% rms]
0	0.05 / -	0.04
0.01	0.08 / -	0.09
0.02	0.13 / -	0.07
0.03	0.27 / -	0.15
0.04	0.39 / -	0.17
0.05	0.53 / -	0.15
0.06	0.61 / 0.13	0.19
0.07	0.69 / 0.27	0.24
0.08	1.03 / 0.39	0.29
0.09	1.21 / 0.27	0.40
0.1	1.37 / 0.39	0.49
0.2	2.96 / 2.03	1.87
0.3	4.31 / 3.52	3.13
0.4	5.48 / 4.80	4.70
0.5	6.52 / 5.91	5.79
0.6	7.46 / 6.93	6.89
0.7	8.33 / 7.82	7.72
0.8	9.15 / 8.66	9.12
0.9	9.93 / 9.46	10.10

B.) **Table of EVM Error Difference between floating-point filter and fixed-point implementations**

EVM Error Difference between Floating-point and Fixed-point Pulse-shaping Filter Implementations		
Alpha	(8-bit) Avg. Error [% rms]/Error Var.	(16-bit) Avg. Error [%rms]/Error Var.
0.1	-0.1986 / 0.0662	0.0004 / 1.44e-4
0.2	-0.4539 / 0.0960	0.0002 / 2.56e-4
0.3	-0.1852 / 0.0250	-7.38e-6 / 1.54e-6
0.4	-0.3438 / 0.0487	-6.36e-6 / 2.61e-6
0.5	-0.2564 / 0.0257	0.0001 / 1.12e-4
0.6	-0.2910 / 0.0251	0.0001 / 1e-6
0.7	-0.2564 / 0.0183	4.34e-5 / 1.69e-6

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