



PLL Testing

- Test Conditions
- Measurements
- Calculations



Disconnect Settings

The screenshot shows the 'PLL_Testing' application window with the 'Disconnect Settings' section selected in the left-hand menu. The main area displays a grid of 'DutControl' settings for various power pins. Each setting is represented by a box with a label and a value.

Label	Value
Vcc 1	0
Vcc 3	0
Vcc 5	0
Vcc 6	0
Device Power 1	open
Device Power 2	open
Device Power 3	open
Device Power 4	open
Device Power 5	open
Device Power 9	open
Device Power 1 0	open
Device Power 1 2	open
Device Power 1 3	open
Device Power 1 4	open



Connect Sequence

The screenshot shows the PLL_Testing software interface. The window title is "PLL_Testing". The menu bar includes File, Edit, Test Plan, Tester, Limits, Options, Help, and Debug. The left sidebar shows a tree view with the following items: Test Plan Settings, Global Defaults, Disconnect Settings, Connect Sequence (highlighted), Test Section: Continuity, Conditional Statement, Section Defaults, Test: Conn_I2C_CLK, and Test: Conn_I2C_SDA. On the right side, there are three buttons: Compile, Run, and Repeat. The main workspace contains a sequence of 14 "DutControl" blocks arranged in three rows. The first row has five blocks: "Device Power 1 4", "Device Power 1 3", "Device Power 1 2", "Device Power 1 0", and "Device Power 9". The second row has five blocks: "Device Power 5", "Device Power 4", "Device Power 3", "Device Power 2", and "Device Power 1". The third row has four blocks: "Vcc 6", "Vcc 5", "Vcc 3", and "Vcc 1". Each block contains a value: "open" for the first two rows and "3.3" for the third row.



Continuity Tests, Section Defaults

PLL_Testing

File Edit Test Plan Tester Limits Options Help Debug

Test Section: Continuity
Conditional Statement
Section Defaults
Test: Conn_I2C_CLK
Test: Conn_I2C_SDA
Test: Conn_MIX2_VCC
Test: Conn_VLNA_VCC
Test Section: Leakage Current
Conditional Statement

Compile
Run
Repeat

DutControl Vcc 1 0	DutControl Device Power 1 open	DutControl Device Power 9 open	StaticDigital Measure I Force -150 u	StaticDigital Measure Mode vMeas	StaticDigital Db 1 open	
DutControl Vcc 2 0	DutControl Device Power 2 open	DutControl Device Power 1 0 open	StaticDigital Measure I Limit -150 u	StaticDigital Measure V Limit -3	StaticDigital Db 2 open	StaticDigital Db 1 4 open
DutControl Vcc 3 0	DutControl Device Power 3 open	DutControl Device Power 1 2 open			StaticDigital Db 3 open	StaticDigital Db 1 5 open
DutControl Vcc 4 0	DutControl Device Power 4 open	DutControl Device Power 1 3 open			StaticDigital Db 4 open	StaticDigital Db 1 6 open
DutControl Vcc 5 0	DutControl Device Power 5 open	DutControl Device Power 1 4 open				
DutControl Vcc 6 0						



Continuity Test for Digital Line: I2C Clock

The screenshot shows the PLL_Testing software interface. The window title is "PLL_Testing". The menu bar includes File, Edit, Test Plan, Tester, Limits, Options, Help, and Debug. The main area is divided into sections:

- Test Section: Continuity**
 - Conditional Statement
 - Section Defaults
 - Test: Conn_I2C_CLK** (highlighted)
 - Test: Conn_I2C_SDA
 - Test: Conn_MIX2_VCC
 - Test: Conn_VLNA_VCC
- Test Section: Leakage Current**
 - Conditional Statement

On the right side, there are three buttons: Compile, Run, and Repeat.

The main workspace contains several configuration blocks:

- StaticDigital** (Measure Pin): DB3
- StaticDigital** (Measure Mode): vMeas
- StaticDigital** (Db 3): open
- StaticDigital** (Measure I Limit): -150 u
- StaticDigital** (Measure V Limit): -3
- StaticDigital** (Measure I Force): -150 u
- System** (Pause): 5000
- StaticDigital** (MEAS): Voltage A
- System** (Save Volts): A Conn_I2C_CLK

A line connects the "Voltage A" block to the "A Conn_I2C_CLK" block.



Continuity Test for Digital Line: I2C Data Read/Write

The screenshot shows the PLL_Testing software interface. The window title is "PLL_Testing". The menu bar includes File, Edit, Test Plan, Tester, Limits, Options, Help, and Debug. The main area is divided into two sections: "Test Section: Continuity" and "Test Section: Leakage Current".

Test Section: Continuity

- Conditional Statement
- Section Defaults
- Test: Conn_I2C_CLK
- Test: Conn_I2C_SDA** (highlighted)
- Test: Conn_MIX2_VCC
- Test: Conn_VLNA_VCC

Test Section: Leakage Current

- Conditional Statement

On the right side of the Continuity section, there are three buttons: Compile, Run, and Repeat.

The main workspace contains several configuration blocks:

- StaticDigital Measure Pin**: DB1
- StaticDigital Measure Mode**: vMeas
- StaticDigital Db 1**: open
- StaticDigital Measure I Force**: -500 u
- StaticDigital Measure V Limit**: -3
- StaticDigital Measure I Limit**: -500 u
- System Pause**: 5000
- PRE MEAS** (Group):
 - StaticDigital Measure Pin**: DB7
 - System Sequence Delay**: 5000
 - StaticDigital Measure Pin**: DB1
- StaticDigital MEAS**: Voltage A
- System Save Volts**: Conn SDA



Continuity Test for Typical VCC Line

The screenshot shows the PLL_Testing software interface. The title bar reads "PLL_Testing". The menu bar includes "File", "Edit", "Test Plan", "Tester", "Limits", "Options", "Help", and "Debug".

The main window is divided into two sections:

- Test Section: Continuity**
 - Conditional Statement
 - Section Defaults
 - Test: Conn_I2C_CLK
 - Test: Conn_I2C_SDA
 - Test: Conn_MIX2_VCC** (highlighted in black)
 - Test: Conn_VLNA_VCC
- Test Section: Leakage Current**
 - Conditional Statement

On the right side of the window, there are three buttons: "Compile", "Run", and "Repeat".

The lower half of the window displays a block diagram of the test setup:

- DutControl** blocks:
 - Device Power 2: Vcc 3
 - Vmeasure: Vcc3
 - Vcc 3 Mode: current
 - Voltage Meas Mode: single
 - Icc 3: -700 u
 - Voltage Meas Max: 3
- MEAS** block: Voltage A
- System** block: Save Volts A Conn MIX2_VCC

A line connects the "A" terminal of the MEAS block to the "A" terminal of the System block.



Continuity Test for Typical VCC Line

The screenshot shows the PLL_Testing software interface. The window title is "PLL_Testing". The menu bar includes File, Edit, Test Plan, Tester, Limits, Options, Help, and Debug. The main area is divided into sections:

- Test Section: Continuity**
 - Conditional Statement
 - Section Defaults
 - Test: Conn_I2C_CLK
 - Test: Conn_I2C_SDA
 - Test: Conn_MIX2_VCC
 - Test: Conn_VLNA_VCC** (highlighted)
- Test Section: Leakage Current**
 - Conditional Statement

On the right side, there are three buttons: Compile, Run, and Repeat.

The main workspace contains a block diagram with the following components and connections:

- DutControl** (top center): Vmeasure → Vcc5
- DutControl** (left): Vcc 5 Mode → current
- DutControl** (middle): Voltage Meas Mode → single
- DutControl** (bottom left): Icc 5 → -0.003
- DutControl** (bottom right): Voltage Meas Max → 3
- DutControl** (right): MEAS → Voltage A
- System** (right): Save Volts → Conn_VLNA_VCC

A connection line links the "Voltage A" output of the MEAS block to the "Conn_VLNA_VCC" input of the Save Volts block.



Leakage Current, Section Defaults Force 0V on each Pin Individually

The screenshot displays the PLL_Testing software interface. The window title is "PLL_Testing". The menu bar includes File, Edit, Test Plan, Tester, Limits, Options, Help, and Debug. The main content area is divided into sections:

- Test Section: Leakage Current**
 - Conditional Statement
 - Section Defaults** (highlighted in black)
 - Test: Leak_I2C_CLK
 - Test: Leak_I2C_EN
- Test Section: I2C Read Registers (Unoptimized)**
 - Conditional Statement
 - Section Defaults**
 - Test: Dev_00

On the right side of the interface, there are three green buttons: **Compile**, **Run**, and **Repeat**.

The bottom section of the interface contains several configuration boxes:

- System**: Averages (5)
- StaticDigital**: Db 3 (open)
- StaticDigital**: Measure V Force (0)
- StaticDigital**: Measure Mode (I meas)
- StaticDigital**: Db 4 (open)
- StaticDigital**: Current Meas Max (-1000 n)
- StaticDigital**: Db 1 4 (open)
- StaticDigital**: Measure I Limit (-1000 n)
- StaticDigital**: Db 1 5 (open)
- StaticDigital**: Db 1 6 (open)



Leakage Current for Digital Pin

The screenshot shows the PLL_Testing software interface. The window title is "PLL_Testing" and the menu bar includes File, Edit, Test Plan, Tester, Limits, Options, Help, and Debug. The main area is divided into two test sections:

- Test Section: Leakage Current**
 - Conditional Statement
 - Section Defaults
 - Test: Leak_I2C_CLK** (highlighted)
 - Test: Leak_I2C_EN
- Test Section: I2C Read Registers (Unoptimized)**
 - Conditional Statement
 - Section Defaults
 - Test: Reg_00

On the right side, there are three green buttons: **Compile**, **Run**, and **Repeat**.

The main workspace contains several configuration blocks:

- StaticDigital Measure Pin**: DB3
- StaticDigital Measure Mode**: Imeas
- StaticDigital Db 3**: open
- StaticDigital Measure V Force**: 0
- StaticDigital Current Meas Max**: -1000 n
- StaticDigital MEAS Current**: A
- System Save Volts**: Leak_I2C_CLK
- System Pause**: 1000
- StaticDigital Measure I Limit**: -1000 n

A red arrow points from the "Current" block to the "Leak_I2C_CLK" block in the "Save Volts" block.



Leakage Current for Control Line

The screenshot shows the PLL_Testing software interface. The menu bar includes File, Edit, Test Plan, Tester, Limits, Options, Help, and Debug. The main window is divided into two sections:

- Test Section: Leakage Current**
 - Conditional Statement
 - Section Defaults
 - Test: Leak_I2C_CLK
 - Test: Leak_I2C_EN** (highlighted)
- Test Section: I2C Read Registers (Unoptimized)**
 - Conditional Statement
 - Section Defaults
 - Test: Dev_00

On the right side, there are three green buttons: **Compile**, **Run**, and **Repeat**.

The main workspace contains several configuration blocks:

- StaticDigital Measure Pin**: DB4
- StaticDigital Measure Mode**: Imeas
- StaticDigital Db 4**: open
- StaticDigital Measure V Force**: 0
- StaticDigital Current Meas Max**: -1000 n
- StaticDigital Measure I Limit**: -1000 n
- System Pause**: 1000
- StaticDigital MEAS**: Current A
- System Save Volts**: Leak_I2C_EN

A line connects the 'Current A' block to the 'Leak_I2C_EN' block.



I2C Read Registers, Section Defaults

The screenshot shows the PLL_Testing software interface. The title bar reads "PLL_Testing". The menu bar includes "File", "Edit", "Test Plan", "Tester", "Limits", "Options", "Help", and "Debug". The main window displays "Test Section: I2C Read Registers (Unoptimized)" and "Conditional Statement". Below this, the "Section Defaults" are listed in red text: "Test: Reg_00", "Test: Reg_01", "Test: Reg_02", "Test: Reg_0A", "Test: Reg_0B", and "Test: Reg_10". On the right side, there are three green buttons: "Compile", "Run", and "Repeat".

The configuration area below the list shows three "StaticDigital" components:

- StaticDigital 1:** Labeled "I 2 C Address", with a value of "1100000". This component is highlighted with a yellow border.
- StaticDigital 2:** Labeled "Voff High Byte", with a value of "0". Below it is "Von High Byte" with a value of "3.3".
- StaticDigital 3:** Labeled "Db 1 5", with a value of "off". Below it is "Db 1 6", with a value of "off".



Read Register 00

The screenshot shows the PLL_Testing software interface. The main window title is "PLL_Testing". The menu bar includes "File", "Edit", "Test Plan", "Tester", "Limits", "Options", "Help", and "Debug". The test plan is titled "Test Section: I2C Read Registers (Unoptimized)". Under "Section Defaults", the following tests are listed:

- Test: Reg_00 (highlighted in black)
- Test: Reg_01
- Test: Reg_02
- Test: Reg_0A
- Test: Reg_0B
- Test: Reg_10

On the right side of the test plan, there are three green buttons: "Compile", "Run", and "Repeat".

Below the test plan, there is a diagram illustrating the test setup. It shows a "StaticDigital" block labeled "I 2 C Register" with a value of "00000000". This block is connected to a "System" block labeled "Save linear" which contains a "Reg00" component. The connection is shown as a line from the "I2C byte A" output of the "StaticDigital" block to the "A" input of the "Reg00" component.



Read Register 01

PLL_Testing

File Edit Test Plan Tester Limits Options Help Debug

Test Section: I2C Read Registers (Unoptimized)

Conditional Statement

Section Defaults

Test: Reg_00

Test: Reg_01

Test: Reg_02

Test: Reg_0A

Test: Reg_0B

Test: Reg_10

Compile

Run

Repeat

StaticDigital

I 2 C Register

00000001

StaticDigital

MEAS

I2C byte A

System

Save linear

Reg01



Read Register 02

PLL_Testing

File Edit Test Plan Tester Limits Options Help Debug

Test Section: I2C Read Registers (Unoptimized)

Conditional Statement

Section Defaults

Test: Reg_00

Test: Reg_01

Test: Reg_02

Test: Reg_0A

Test: Reg_0B

Test: Reg_10

Compile

Run

Repeat

StaticDigital

I 2 C Register

00000010

StaticDigital

MEAS

I2C byte A

System

Save linear

Reg02



Read Register 0A

PLL_Testing

File Edit Test Plan Tester Limits Options Help Debug

Test Section: I2C Read Registers (Unoptimized)

Conditional Statement

Section Defaults

Test: Reg_00

Test: Reg_01

Test: Reg_02

Test: Reg_0A

Test: Reg_0B

Test: Reg_10

Compile

Run

Repeat

StaticDigital

I 2 C Register

00001010

StaticDigital

MEAS

I2C byte A

System

Save linear

A Reg0A



Read Register 0B

The screenshot shows the PLL_Testing software interface. The main window title is "PLL_Testing" and it has a menu bar with "File", "Edit", "Test Plan", "Tester", "Limits", "Options", "Help", and "Debug". The test section is "I2C Read Registers (Unoptimized)". The test list includes "Test: Reg_00", "Test: Reg_01", "Test: Reg_02", "Test: Reg_0A", and "Test: Reg_0B" (highlighted in blue). On the right, there are three green buttons: "Compile", "Run", and "Repeat".

Below the test list is a diagram illustrating the data flow. It consists of three main components:

- StaticDigital (I2C Register):** A box containing the binary value "00001011". This box is highlighted with a yellow border.
- StaticDigital (MEAS):** A box labeled "MEAS" containing "I2C byte A".
- System (Save linear):** A box labeled "Save linear" containing "Reg0B".

Arrows indicate the data flow: from the "I2C Register" box to the "MEAS" box, and from the "MEAS" box to the "Reg0B" box.



Read Register 10

The screenshot shows the PLL_Testing software interface. The window title is "PLL_Testing" and the menu bar includes "File", "Edit", "Test Plan", "Tester", "Limits", "Options", "Help", and "Debug".

Section Defaults

- Test: Reg_00
- Test: Reg_01
- Test: Reg_02
- Test: Reg_0A
- Test: Reg_0B
- Test: Reg_10** (highlighted in black)
- Test: Reg_11
- Test Section: (Unoptimized)

On the right side of the interface, there are three green buttons: "Compile", "Run", and "Repeat".

Block Diagram:

- A yellow box highlights a "StaticDigital" block labeled "I 2 C Register" containing the value "00010000".
- Below it, another "StaticDigital" block labeled "MEAS" contains "I2C byte A".
- To the right, a "System" block labeled "Save linear" contains "Reg10".
- A line connects the "A" output of the "MEAS" block to the "A" input of the "Reg10" block.



Read Register 11

The screenshot shows the PLL_Testing software interface. The menu bar includes File, Edit, Test Plan, Tester, Limits, Options, Help, and Debug. The main window is titled "Section Defaults" and lists several test configurations: Test: Reg_00, Test: Reg_01, Test: Reg_02, Test: Reg_0A, Test: Reg_0B, Test: Reg_10, and Test: Reg_11. The "Test: Reg_11" entry is highlighted in blue. To the right of the list are three green buttons: Compile, Run, and Repeat. Below the list, a block diagram is displayed. It consists of three main components: a "StaticDigital" block labeled "I 2 C Register" containing the value "00010001", a "StaticDigital" block labeled "MEAS" containing "I2C byte A", and a "System" block labeled "Save linear" containing "Reg11". A line connects the "I2C byte A" output of the MEAS block to the "A" input of the Reg11 block.



Icc Measurements, Section Defaults

The screenshot displays the PLL_Testing software interface. The window title is "PLL_Testing". The menu bar includes "File", "Edit", "Test Plan", "Tester", "Limits", "Options", "Help", and "Debug". The main content area is titled "Test Section: Icc (Unoptimized)" and contains a "Conditional Statement" section. Underneath, the "Section Defaults" are listed in red text: "Test: Init Part", "Test: Icc_Mix2", "Test: Icc_FIT", "Test: Icc_I2C", "Test: Icc_RFLT", and "Test: Icc_VLNA". To the right of the list are three green buttons: "Compile", "Run", and "Repeat". Below the list, there are three "DutControl" blocks, each with a "Vcc" value in a box: "Vcc 2" with "3.3", "Vcc 4" with "3.3", and "Device Power 6" with "Vcc 3".



Typical Way to Initialize Part, Remove Vcc, wait, Add Vcc

The screenshot shows the PLL_Testing software interface. The window title is "PLL_Testing" and the menu bar includes File, Edit, Test Plan, Tester, Limits, Options, Help, and Debug. The main area displays a test section titled "Test Section: lcc (Unoptimized)". Underneath, there are several test items listed: "Test: Init Part" (highlighted in black), "Test: lcc_Mix2", "Test: lcc_F1T", "Test: lcc_I2C", "Test: lcc_RFLT", and "Test: lcc_VLNA". To the right of the test list are three green buttons: "Compile", "Run", and "Repeat". Below the test list, there is a "Pre Meas" section with three "DutControl" blocks. The first block is labeled "DutControl" and contains "Device Power 1 2" with a value of "open". The second block is labeled "System" and contains "Sequence Delay" with a value of "1000". The third block is labeled "DutControl" and contains "Device Power 1 2" with a value of "Vcc 1". Below these blocks, there is another "DutControl" block labeled "MEAS" containing "Voltage A".



Typical Icc Measurement

The screenshot displays the PLL_Testing software interface. The menu bar includes File, Edit, Test Plan, Tester, Limits, Options, Help, and Debug. The main window shows a test section titled "Test Section: Icc (Unoptimized)". The test list includes: Conditional Statement, Section Defaults, Test: Init Part, Test: Icc_Mix2 (highlighted), Test: Icc_FIT, Test: Icc_I2C, Test: Icc_RFLT, and Test: Icc_MINA. On the right side, there are three green buttons: Compile, Run, and Repeat.

The configuration area is divided into three sections:

- DutControl**: Contains a box for "Device Power 1" with a sub-box for "Vcc 4".
- DutControl**: Contains a "MEAS" box with "Current A" and a "Current Meas Max" box with the value "0.1". Below these is an "Imeasure" box with the value "Vcc4".
- System**: Contains a "Save Amps" box with "Icc Mix2".

A line connects the "Current A" box in the second DutControl section to the "Icc Mix2" box in the System section, indicating the measurement point.



Icc for I2C Supply Line

The screenshot shows the PLL_Testing software interface. The window title is "PLL_Testing" and the menu bar includes File, Edit, Test Plan, Tester, Limits, Options, Help, and Debug. The main area displays the "Test Section: Icc (Unoptimized)" with a list of tests: Conditional Statement, Section Defaults, Test: Init Part, Test: Icc_Mix2, Test: Icc_F1T, Test: Icc_I2C (highlighted), Test: Icc_RFLT, and Test: Icc_VI_MA. On the right side, there are three green buttons: Compile, Run, and Repeat. Below the test list, there is a block diagram showing the test setup. It includes a "DutControl" block for "Device Power 1 2" with a "Vcc 2" input. Another "DutControl" block for "MEAS" contains a "Current A" measurement point, a "Current Meas Max" set to "0.1", and an "Imeasure" set to "Vcc2". A "System" block for "Save Amps" contains an "Icc I2C" measurement point. A line connects the "Current A" measurement point to the "Icc I2C" measurement point.



Charge Pump Section Defaults

The screenshot shows the PLL_Testing software interface. The menu bar includes File, Edit, Test Plan, Tester, Limits, Options, Help, and Debug. The main window displays the 'Test Section: Charge Pumps' section, which is currently selected. Below this, the 'Section Defaults' are listed: 'Test: CP1 src', 'Test: CP1 sink', and 'Test: CP1 both'. Below the defaults, the 'Test Section: LO Locked' section is visible, also showing 'Section Defaults'. On the right side of the window, there are three green buttons: 'Compile', 'Run', and 'Repeat'. The main workspace contains several test blocks arranged in a grid:

- Dut** block: T S T C P, CP test
- DutControl** block: Device Power 7, Vcc 4
- DutControl** block: Imeasure, Vcc4
- Dut** block: L 1 A C P, CP1 man
- DutControl** block: Vcc 4, 2.1
- DutControl** block: Imeasure Bw, slow



Charge Pump Source Current

The screenshot shows a software window titled "PLL_Testing" with a menu bar (File, Edit, Test Plan, Tester, Limits, Options, Help, Debug). The main area is divided into two sections:

- Test Section: Charge Pumps**
 - Conditional Statement
 - Section Defaults
 - Test: CP1 src** (highlighted)
 - Test: CP1 sink
 - Test: CP1 both
- Test Section: LO Locked**
 - Conditional Statement
 - Section Defaults

On the right side, there are three green buttons: **Compile**, **Run**, and **Repeat**.

The lower half of the window displays a block diagram with the following components:

- Dut** (Top Left): A box containing "T U P" and a sub-box "CP's src".
- DutControl** (Top Right): A box containing "Current Meas Max" and a sub-box "700 u".
- Dut** (Bottom Left): A box containing "T D W N" and a sub-box "CP's norm".
- DutControl** (Bottom Middle): A box containing "MEAS" and a sub-box "Current A".
- System** (Bottom Right): A box containing "Save Amps" and a sub-box "A CP1 src".

A line connects the "Current A" box in the bottom middle "DutControl" to the "A CP1 src" box in the "System" box.



Charge Pump Sink Current

The screenshot shows a software window titled "PLL_Testing" with a menu bar containing "File", "Edit", "Test Plan", "Tester", "Limits", "Options", "Help", and "Debug". The main area is divided into two sections:

- Test Section: Charge Pumps**
 - Conditional Statement
 - Section Defaults
 - Test: CP1 src
 - Test: CP1 sink** (highlighted)
 - Test: CP1 both
- Test Section: L0 Locked**
 - Conditional Statement
 - Section Defaults

On the right side of the window, there are three green buttons: "Compile", "Run", and "Repeat".

The main workspace contains a block diagram with the following components:

- Dut** (top left): A box containing "T U P" and "CP's norm".
- DutControl** (top middle): A box containing "Current Meas Max" and "700 u".
- Dut** (bottom left): A box containing "T D W N" and "CP's sink".
- DutControl** (bottom middle): A box containing "MEAS" and "Current A".
- System** (bottom right): A box containing "Save Amps" and "A CP1 sink".

A line connects the "Current A" output of the bottom middle "DutControl" block to the "A CP1 sink" input of the "System" block.



Testing Both Charge Pump Sink & Source Current

The screenshot shows the PLL_Testing software interface. The window title is "PLL_Testing" and the menu bar includes File, Edit, Test Plan, Tester, Limits, Options, Help, and Debug. The main area is divided into two sections: "Test Section: Charge Pumps" and "Test Section: LO Locked". Under "Test Section: Charge Pumps", there are three test items: "Conditional Statement", "Section Defaults", and "Test: CP1 src", "Test: CP1 sink", and "Test: CP1 both". The "Test: CP1 both" item is highlighted. To the right of the test sections are three green buttons: "Compile", "Run", and "Repeat".

Below the test sections is a block diagram. It consists of several blocks:

- A "Dut" block labeled "T U P" containing "CP's src".
- A "DutControl" block labeled "Current Meas Max" containing "50 u".
- A "Dut" block labeled "T D W N" containing "CP's sink".
- A "DutControl" block labeled "MEAS" containing "Current A".
- A "System" block labeled "Save Amps" containing "A CP1 both".

Connections in the diagram include a line from the "Current A" block to the "A CP1 both" block, and a line from the "CP's sink" block to the "MEAS" block.



LO Locked Section Defaults

The screenshot shows the PLL_Testing software interface. The window title is "PLL_Testing" and it has a menu bar with "File", "Edit", "Test Plan", "Tester", "Limits", "Options", "Help", and "Debug".

The main content area displays two test sections:

- Test Section: LO Locked**
Conditional Statement
Section Defaults
Test: Check if LO is Locked (returns 32 if locked, 0 if unlocked)
- Test Section: Measuring Filter and Computing Spline Fit (Unoptimized)**
Conditional Statement
Section Defaults
Test: Measure 5 evenly spaced Points, use data for calculating Curve
Test: Calc Spline

On the right side of the interface, there are three green buttons: "Compile", "Run", and "Repeat".

The bottom section of the interface shows hardware configuration blocks:

- Dut**: FM 1 L O, Normal
- DutControl**: Vcc 4, 2.5
- Fixture**: Head Rf 4, DutRf12dB
- Source1**: Rf State, ON
- System**: Averages, 1
- Fixture**: Head Rf 3, DutRf10



Reading Back the Lock Detect Bit Using Modulo to Look at a Single Bit in the Register Byte

PLL_Testing

File Edit Test Plan Tester Limits Options Help Debug

Test Section: L0 Locked
Conditional Statement
Section Defaults
Test: Check if L0 is Locked (returns 32 if locked, 0 if unlocked)

Test Section: Measuring Filter and Computing Spline Fit (Unoptimized)
Conditional Statement
Section Defaults
Test: Measure 5 evenly spaced Points, use data for calculating Curve
Test: Calc Spline

Compile
Run
Repeat

The diagram illustrates the logic for checking the L0 Locked bit. It starts with an I2C Register block (StaticDigital) containing the value 00001000. This value is read by a MEAS block (StaticDigital) labeled 'I2C byte'. The output of the MEAS block is processed by a TYPE CHANGE block (System) labeled 'RiReadD'. The output of this block is then processed by a CALC INPUT block (System) labeled '64.0'. The output of this block is processed by a CALC block (System) labeled 'a modulo b', which is highlighted in yellow. The output of this block is then processed by another CALC INPUT block (System) labeled '32.0'. The output of this block is processed by another CALC block (System) labeled 'a modulo b', which is also highlighted in yellow. The output of this block is then processed by a CALC block (System) labeled 'a - b'. The output of this block is finally processed by a Save linear block (System) labeled 'L0_Locked'.



Curve Fit Section Defaults

The screenshot shows the PLL_Testing software interface. The title bar reads "PLL_Testing". The menu bar includes "File", "Edit", "Test Plan", "Tester", "Limits", "Options", "Help", and "Debug". The main window title is "Test Section: Measuring Filter and Computing Spline Fit (Unoptimized)". Below this, there are sections for "Conditional Statement" and "Section Defaults". The "Section Defaults" section lists several test configurations in red text:

- Test: Measure 5 evenly spaced Points, use data for calculating Curve
- Test: Calc Spline
- Test: Calc Curve, stop = # of lock steps, points = last LO freq - first L
- Test: Slope, new
- Test: Calc Zero Slope point
- Test: Calc Max Power and Max Power Index

On the right side of the window, there are three green buttons: "Compile", "Run", and "Repeat".

The main area of the window contains several control panels for different components:

- Dut**: FM 1 L O, Normal
- DutControl**: Vcc 4, 2.5
- Fixture**: Head Rf 4, DutRf12dB
- Source1**: Rf State, ON
- System**: Averages, 1
- Fixture**: Head Rf 3, DutRf10



Only 5 Data Points Needed to Create Spline Curve Fit

PLL_Testing

File Edit Test Plan Tester Limits Options Help Debug

Test Section: Measuring Filter and Computing Spline Fit (Unoptimized)

Conditional Statement

Section Defaults

Test: Measure 5 evenly spaced Points, use data for calculating Curve

Test: Calc Spline

Test: Calc Curve, stop = # of lock steps, points = last LO freq - first L

Test: Slope, new

Test: Calc Zero Slope point

Test: Calc Max Deviation and Max Deviation Index

Compile

Run

Repeat

System Index	1.1 Hz	1.1 Hz	1.2 Hz	1.2 Hz	1.2 Hz	1.2 Hz
1	112	2	69	1	122	0
2	115	0	71	1	64	0
3	116	14	72	1	0	0
4	112	12	75	0	102	0
5	120	10	77	0	122	0



Calculate the Spline Algorithm using the Spline Calc

The screenshot displays the PLL_Testing software interface. The title bar reads "PLL_Testing". The menu bar includes "File", "Edit", "Test Plan", "Tester", "Limits", "Options", "Help", and "Debug". The main window shows a test section titled "Test Section: Measuring Filter and Computing Spline Fit (Unoptimized)". The test plan includes the following steps:

- Conditional Statement
- Section Defaults
- Test: Measure 5 evenly spaced Points, use data for calculating Curve
- Test: Calc Spline** (highlighted in black)
- Test: Calc Curve, stop = # of lock steps, points = last LO freq - first L
- Test: Slope, new
- Test: Calc Zero Slope point
- Test: Calc Max Deviation and Max Deviation Index

On the right side of the test plan, there are three green buttons: "Compile", "Run", and "Repeat".

Below the test plan is a block diagram showing the system architecture. The diagram consists of several blocks:

- A "System" block labeled "LOCAL VAR SOURCE" containing a "FIFP_Pout" block.
- A "System" block labeled "LOCAL VAR SOURCE" containing a "FIFP_Freq" block.
- A "System" block labeled "CALC" containing a "spline" block. This block is highlighted with a yellow border. It has two input ports labeled "A" and "B".
- A "System" block labeled "LOCAL VAR SAVE" containing a "spline" block. It has an output port labeled "A".
- A "System" block labeled "MEAS" containing a "Calculation only" block.

Connections are shown between the "FIFP_Pout" and "FIFP_Freq" blocks to the "CALC" block's "A" and "B" ports, and from the "LOCAL VAR SAVE" block's "A" port to the "MEAS" block.



Create an Array of Data "Curve" with Data Points every 1 MHz from the Spline Algorithm

PLL_Testing

File Edit Test Plan Tester Limits Options Help Debug

Test Section: Measuring Filter and Computing Spline Fit (Unoptimized)

Conditional Statement

Section Defaults

Test: Measure 5 evenly spaced Points, use data for calculating Curve

Test: Calc Spline

Test: Calc Curve, stop = # of lock steps, points = last LO freq - first L

Test: Slope, new

Test: Calc Zero Slope point

Test: Calc Max Deviation and Max Deviation Index

Compile

Run

Repeat

System

MEAS

Calculation only

Source1

Rf State

OFF

System

LOCAL VAR SOURCE

spline A

System

INSTR STATE SOURCE

Index A

System

CALC

value at index b A

System

Save dbm

curve A

System

Indexed by Index

curve A

System

Index

start

1

stop

5

points

121



Using the deltas Calculation, Create a Slope Array. The new Array is the Slope of the Curve at every data point.

The screenshot shows the PLL_Testing software interface. The window title is "PLL_Testing" and the menu bar includes "File", "Edit", "Test Plan", "Tester", "Limits", "Options", "Help", and "Debug". The main area displays a test plan for "Measuring Filter and Computing Spline Fit (Unoptimized)". The test plan includes several steps, with "Test: Slope, new" highlighted in blue. To the right of the test plan are three green buttons: "Compile", "Run", and "Repeat".

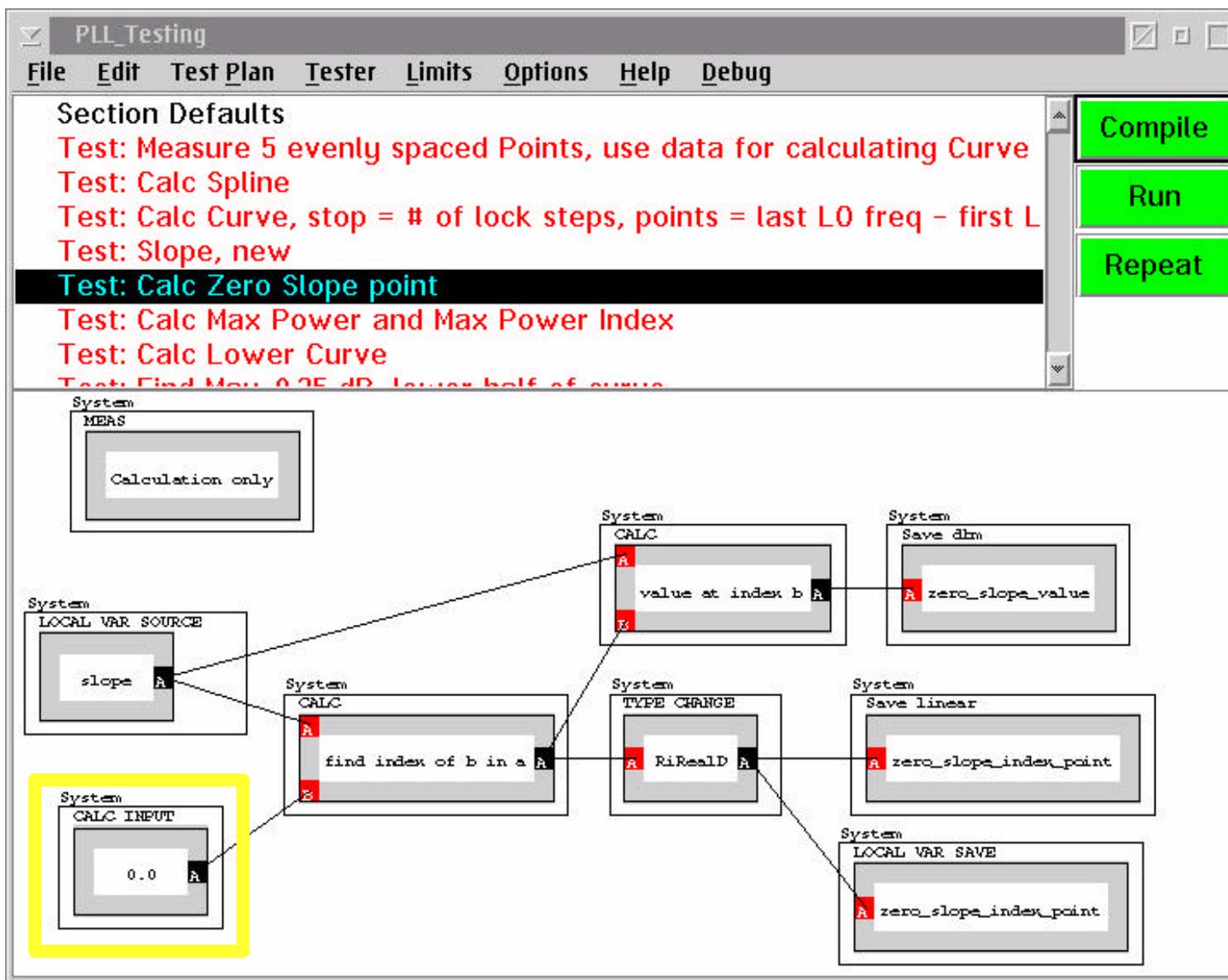
Below the test plan is a block diagram. The diagram consists of several blocks connected in a sequence. The blocks are:

- System LOCAL VAR SOURCE (curve)
- System TYPE CHANGE (Ri PowerDbm)
- System CALC (deltas) - This block is highlighted with a yellow border.
- System LOCAL VAR SAVE (slope)

There is also a separate block labeled "System MEAS" containing "Calculation only".



Calculate the Zero Slope Index Point for the Slope Array





Find the Curve's Maximum Power Value and the Index Point for the Maximum Power Value

PLL_Testing

File Edit Test Plan Tester Limits Options Help Debug

Section Defaults

- Test: Measure 5 evenly spaced Points, use data for calculating Curve
- Test: Calc Spline
- Test: Calc Curve, stop = # of lock steps, points = last LO freq - first L
- Test: Slope, new
- Test: Calc Zero Slope point
- Test: Calc Max Power and Max Power Index**
- Test: Calc Lower Curve
- Test: Find Max 0.25 dB lower half of curve

Compile

Run

Repeat

```
graph LR; subgraph "System LOCAL VAR SOURCE"; direction TB; curve; end; subgraph "System CALC"; direction TB; max_value["max Value"]; max_index["max Index"]; end; subgraph "System LOCAL VAR SOURCE"; direction TB; curve2["curve"]; end; subgraph "System LOCAL VAR SAVE"; direction TB; RiPowerDbm; FIFFF_Max_Pwr_Index; FIFFF_Max_Pwr_index; end; subgraph "System MEAS"; direction TB; Calculation_only["Calculation only"]; end; curve --> max_value; max_value --> RiPowerDbm; RiPowerDbm --> FIFFF_Max_Pwr; curve2 --> max_index; max_index --> FIFFF_Max_Pwr_Index; FIFFF_Max_Pwr_Index --> FIFFF_Max_Pwr_index;
```



Extract the Data Points for the Lower Part of the Curve (From the 1st Data Point to the Maximum Data Point)

The screenshot shows the PLL_Testing software interface. The top menu bar includes File, Edit, Test Plan, Tester, Limits, Options, Help, and Debug. A list of tests is displayed, with "Test: Calc Lower Curve" highlighted in blue. To the right of the list are three green buttons: Compile, Run, and Repeat.

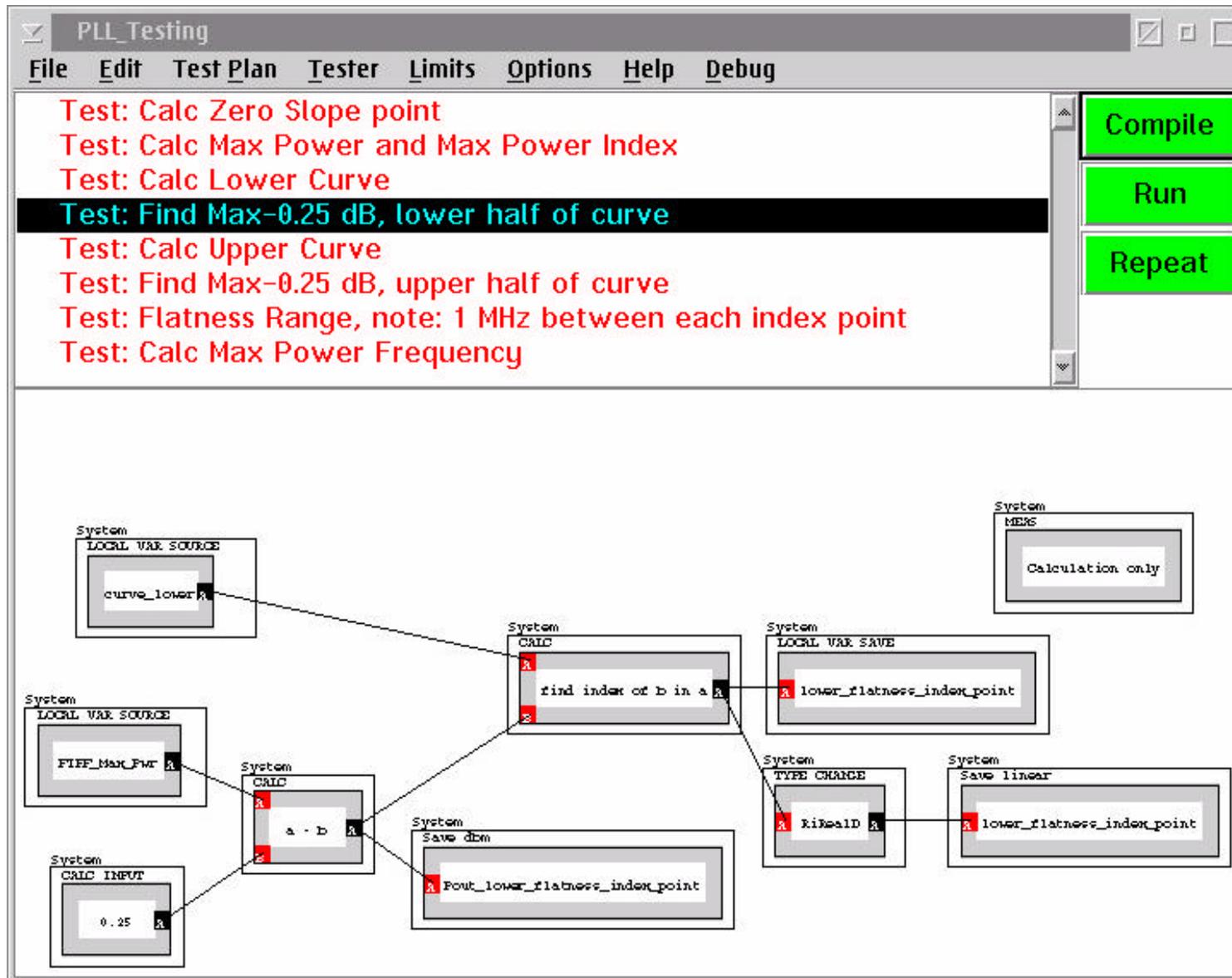
Below the test list is a block diagram illustrating the data extraction process. It consists of several interconnected blocks:

- LOCAL VAR SOURCE** (top left): Contains the text "FIF Max Pwr Index" and a small box labeled "A".
- LOCAL VAR SOURCE** (middle left): Contains the text "curve" and a small box labeled "A".
- CALC INPUT** (bottom left): Contains the text "1.0" and a small box labeled "A".
- CALC** (center): Contains the text "Extract from A to C" and three small boxes labeled "A", "B", and "C".
- LOCAL VAR SAVE** (middle right): Contains the text "curve_lower" and a small box labeled "A".
- MEAS** (top right): Contains the text "Calculation only".

Arrows indicate the flow of data: from the "LOCAL VAR SOURCE" (top left) and "LOCAL VAR SOURCE" (middle left) blocks to the "CALC" block; from the "CALC INPUT" block to the "CALC" block; and from the "CALC" block to the "LOCAL VAR SAVE" block. The "MEAS" block is also connected to the "CALC" block.



Find the Data Point which is 0.25 dB less than the Maximum Data Point in the Lower Curve





Extract the Data Points for the Upper Part of the Curve (From the Maximum Data Point to the Last Data Point)

The screenshot shows the PLL_Testing software interface. The menu includes the following tests:

- Test: Calc Zero Slope point
- Test: Calc Max Power and Max Power Index
- Test: Calc Lower Curve
- Test: Find Max-0.25 dB, lower half of curve
- Test: Calc Upper Curve** (highlighted)
- Test: Find Max-0.25 dB, upper half of curve
- Test: Flatness Range, note: 1 MHz between each index point
- Test: Calc Max Power Frequency

On the right side, there are three green buttons: **Compile**, **Run**, and **Repeat**.

The block diagram below illustrates the 'Calc Upper Curve' test setup:

- System CALC INPUT**: Contains the value 121.0, connected to input A of the **System CALC** block.
- System LOCAL VAR SOURCE**: Contains the variable 'curve', connected to input A of the **System CALC** block.
- System LOCAL VAR SOURCE**: Contains the variable 'F1FF_Max_Pwr_Index', connected to input B of the **System CALC** block.
- System CALC**: Contains the instruction 'Extract from A to C', with inputs A and B, and output C.
- System LOCAL VAR SAVE**: Contains the variable 'curve_upper', connected to output A of the **System CALC** block.
- System MEAS**: Contains the text 'Calculation only'.



Find the Data Point which is 0.25 dB less than the Maximum Data Point in the Upper Curve

PLL_Testing

File Edit Test Plan Tester Limits Options Help Debug

Test: Calc Zero Slope point
Test: Calc Max Power and Max Power Index
Test: Calc Lower Curve
Test: Find Max-0.25 dB, lower half of curve
Test: Calc Upper Curve
Test: Find Max-0.25 dB, upper half of curve
Test: Flatness Range, note: 1 MHz between each index point
Test: Calc Max Power Frequency

Compile
Run
Repeat

```
graph TD
    subgraph "LOCAL VAR SOURCE"
        A[curve_upper]
        B[FREQ_Max_Pwr]
        C[FREQ_Max_Pwr_Index]
    end
    subgraph "CALC"
        D[find index of b in a]
        E[RINDEX]
        F[a + b]
        G[a - b]
    end
    subgraph "LOCAL VAR SOURCE"
        H[0.25]
        I[1.0]
    end
    subgraph "LOCAL VAR SAVE"
        J[upper_flatness_index_point]
        K[upper_flatness_index_point]
    end
    subgraph "Save linear"
        L[upper_flatness_index_point]
    end
    subgraph "Save db"
        M[out_upper_flatness_index_point]
    end
    A --> D
    B --> D
    D --> E
    E --> F
    F --> G
    H --> G
    I --> G
    G --> J
    J --> K
    K --> L
    L --> M
```



Calculate Flatness Range for Curve

PLL_Testing

File Edit Test Plan Tester Limits Options Help Debug

Test: Calc Zero Slope point
Test: Calc Max Power and Max Power Index
Test: Calc Lower Curve
Test: Find Max-0.25 dB, lower half of curve
Test: Calc Upper Curve
Test: Find Max-0.25 dB, upper half of curve
Test: Flatness Range, note: 1 MHz between each index point
Test: Calc Max Power Frequency

Compile
Run
Repeat

```
graph LR; U[LOCAL VAR SOURCE: upper_flatness_index_point] --> C1[CALC: a - b]; L[LOCAL VAR SOURCE: lower_flatness_index_point] --> C1; C1 --> C2[CALC: a + b]; I[CALC INPUT: 1.0] --> C2; C2 --> T[TYPE CHANGE: Ri.FreqD]; T --> S[Save MHz: Flatness_Range];
```



Calculate the Maximum Power Frequency Value for the Entire Curve

