Agenda

- New Capabilities
- New Fixture Modules
- New Calculations and New Buttons
- Local Variables and Disconnect Settings
- Using Connect Sequence & Pre/Post Measure Groups
- New Optimizer Capabilities
- I2C Read, Write, Extracting Data and Fixture Digital
- New Techniques for Modulated and/or Pulsed Signals

New Capabilities

- Fast Frequency Moves: 3x to 20x faster
- Low Current Measurements: down to <1 nA
- New High Speed ARB: up to 40 MHz Clock
- BER: up to 10 MHz
- RF Pulse Profiling: down to 100 nsec resolution
- IQ Meter: +/-0.1 deg. & +/-0.1 dB
- Fixture Digital: up to 60 Mbits/sec.
- High Current Pulse Measurements
- New Test Plan Optimizer Features: Show test times
- Digital Subsystem: 96 pins and 100 MHz Data rates

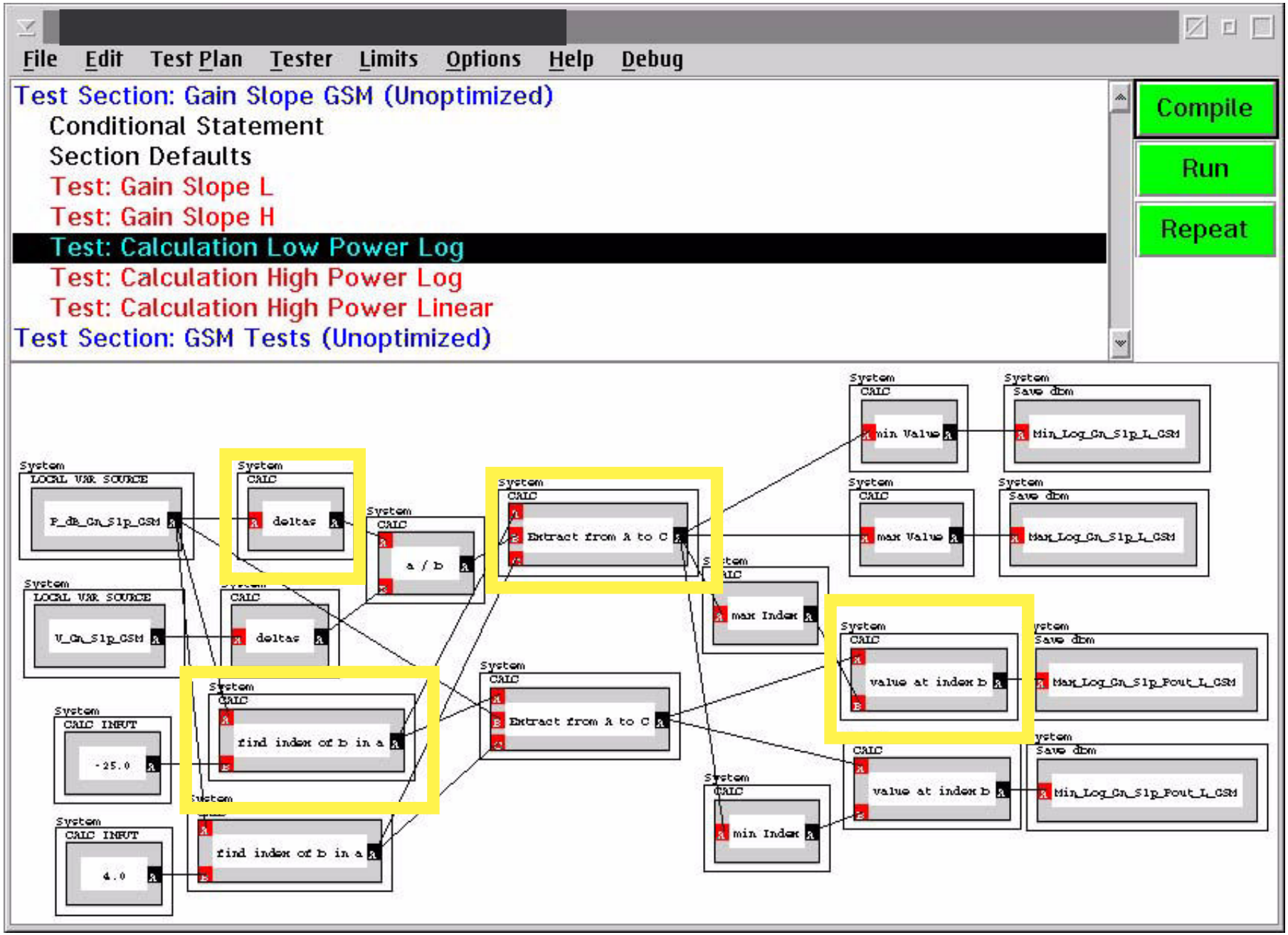
New Fixture Modules

- Low Frequency Noise Source: Noise to <1 MHz
- Delay Line Discriminator: Phase Noise Testing
- Attenuator Module: 3 to 33 dB attenuation, 2 dB steps
- Frequency Divider Module: Divide Ratios: 64, 128 & 256

New Calculations

- Find index of b in a
- Value at index b
- Extract from A to C
- Deltas
- Modulo

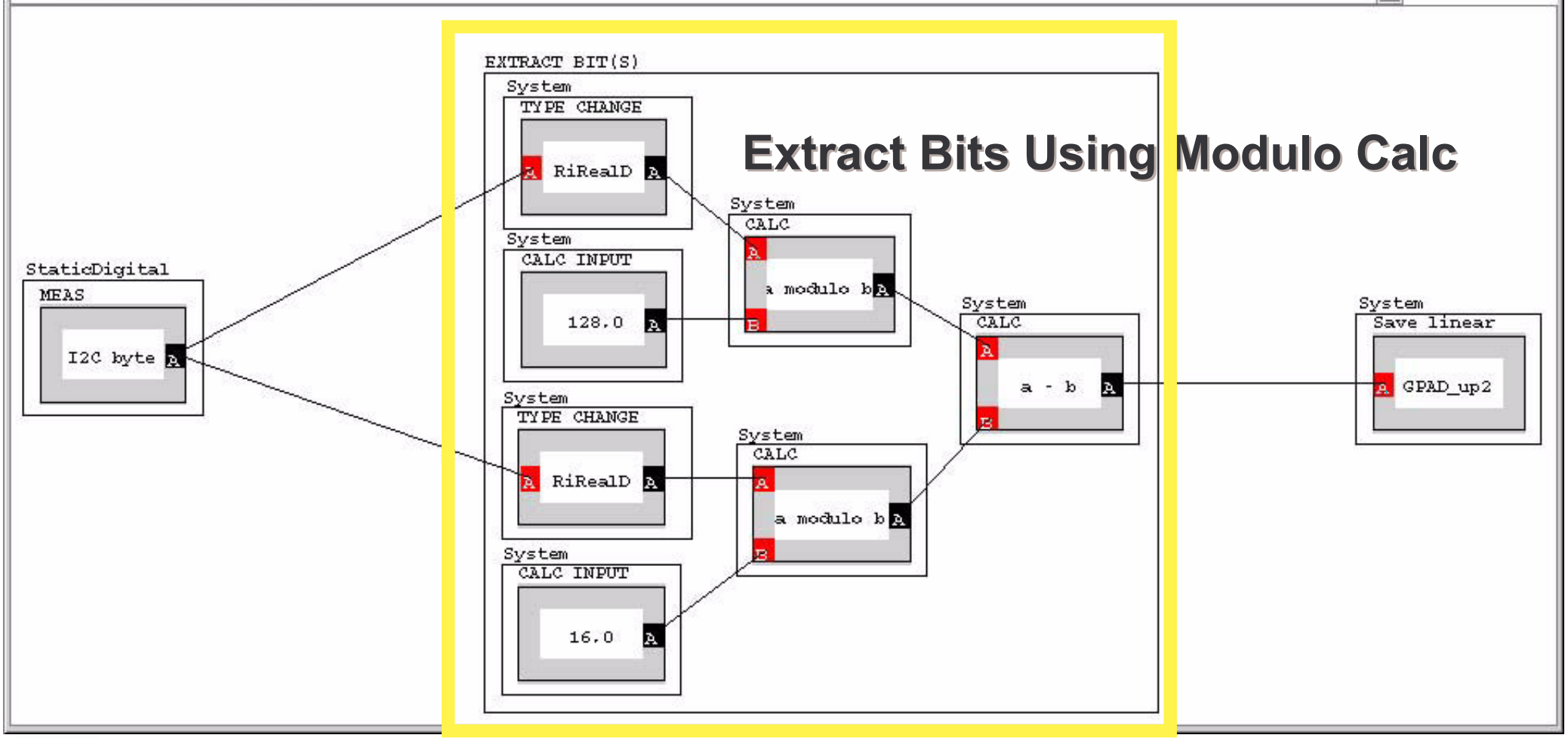
Calc Gain Slope using Deltas, Extract, Find Index & Value at Index



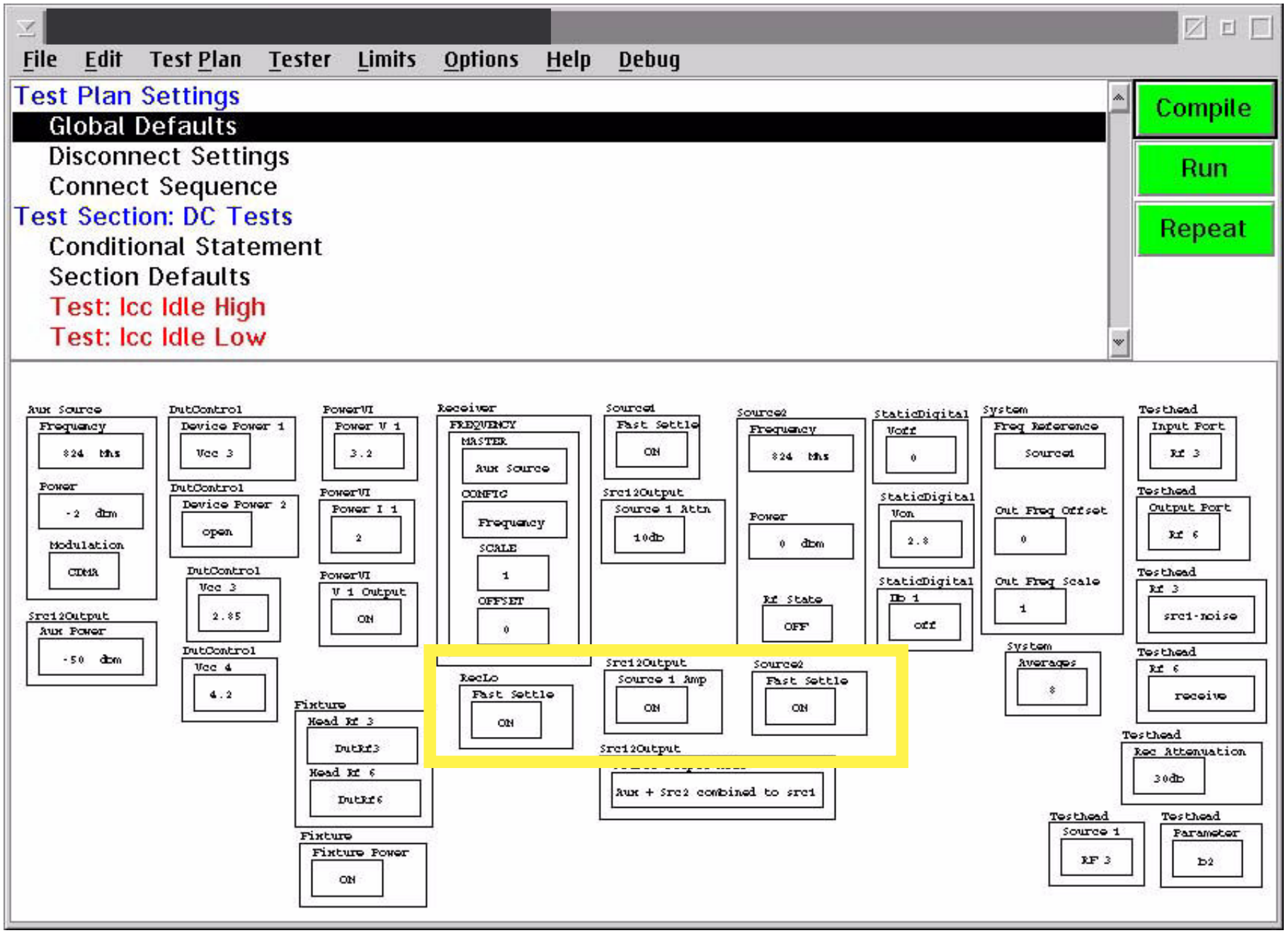
File Edit Test Plan Tester Limits Options Help Debug

Test Section: A/D's Chk (Unoptimized)
Conditional Statement
Section Defaults
Test: A/D enable
Test: GPAD_up_pt1
Test: GPAD_up_pt2
Test: Test
Test: GPAD_up_pt3
Test: GPAD_up_pt4
Test: GPAD_dn_pt4
Test: GPAD_dn_pt3

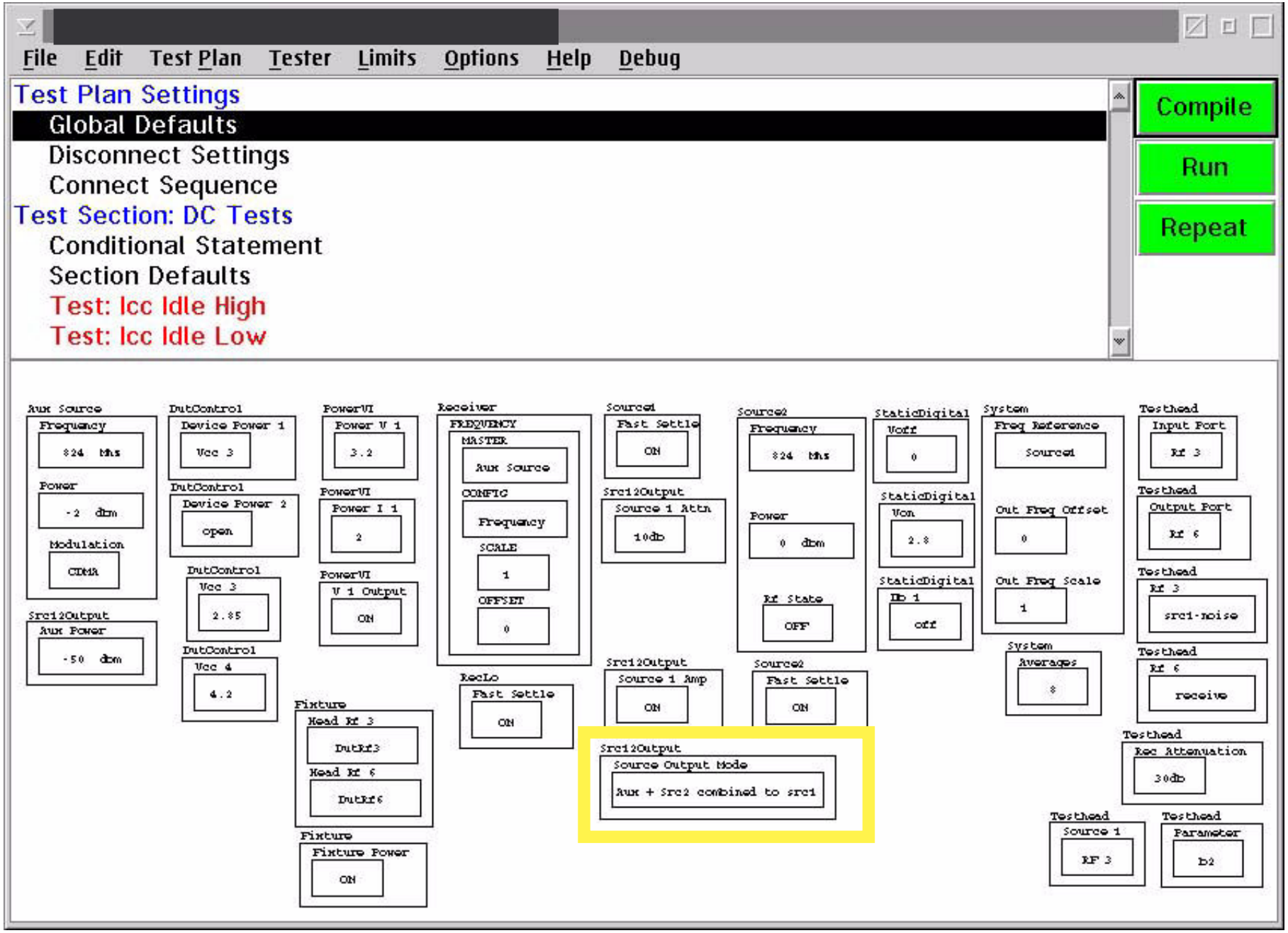
Compile
Run
Repeat



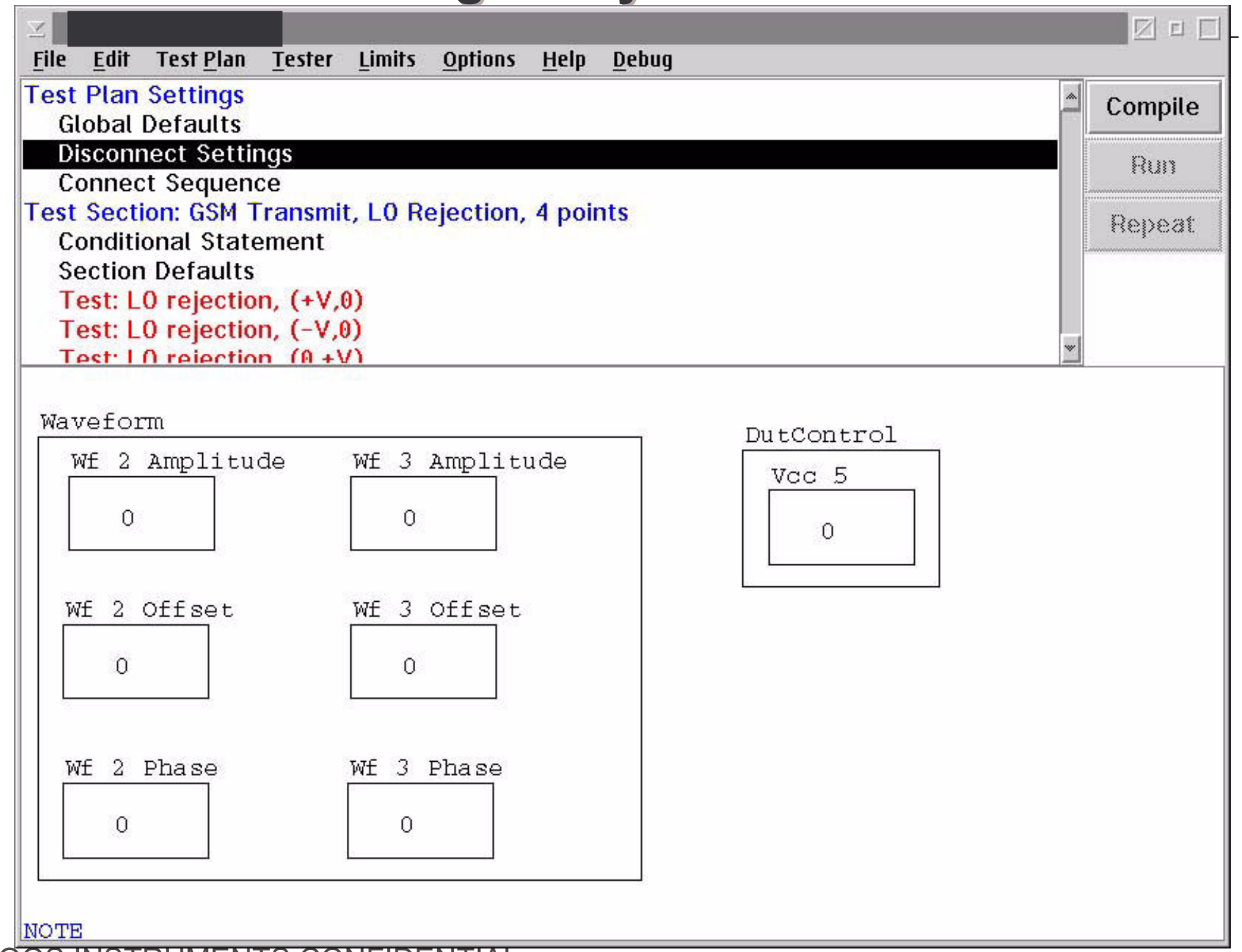
Global Defaults for Source 1, 2 & Receiver LO Fast Settle



Global Default Setting for Scr12Output: Aux + Src2 combined to Src1

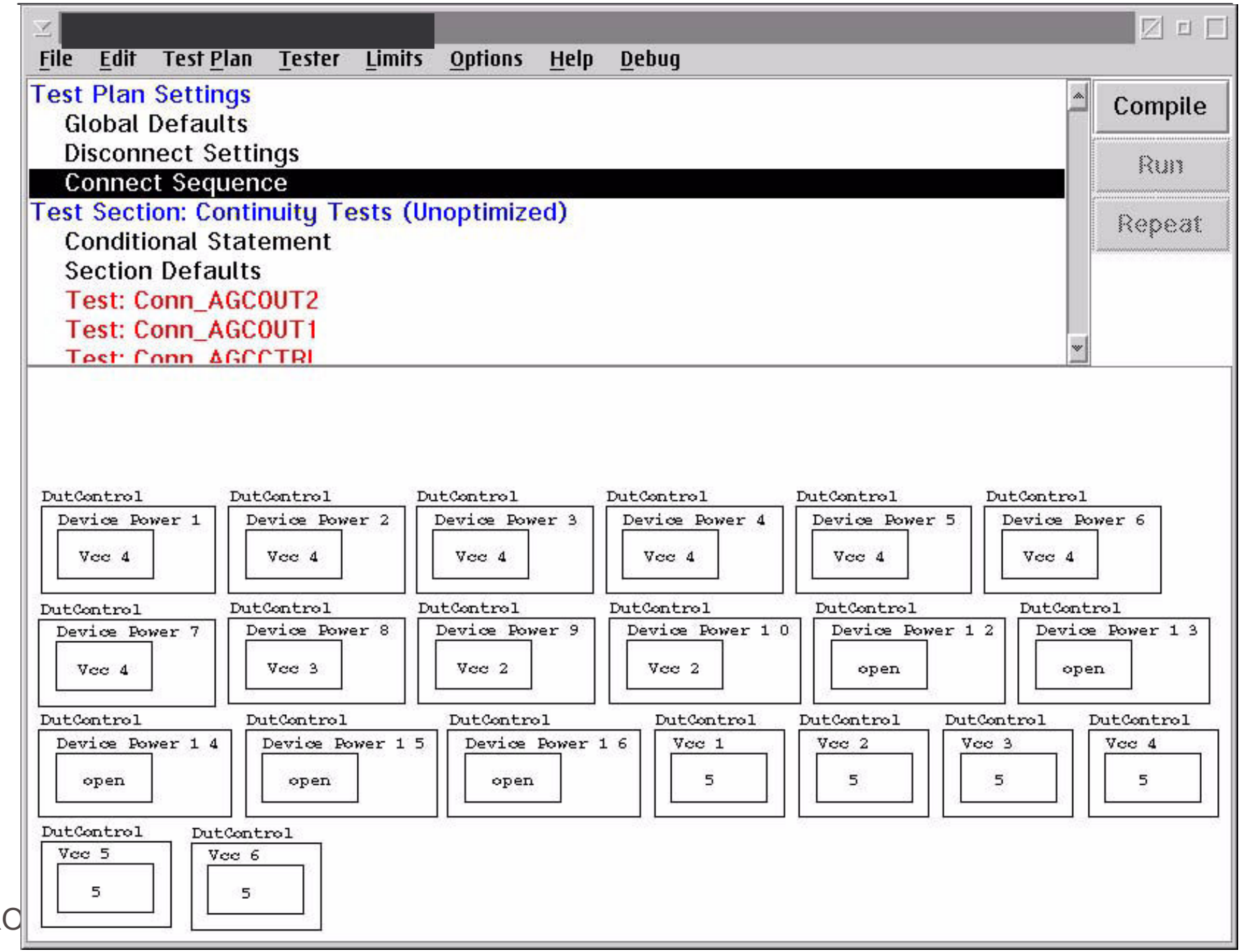


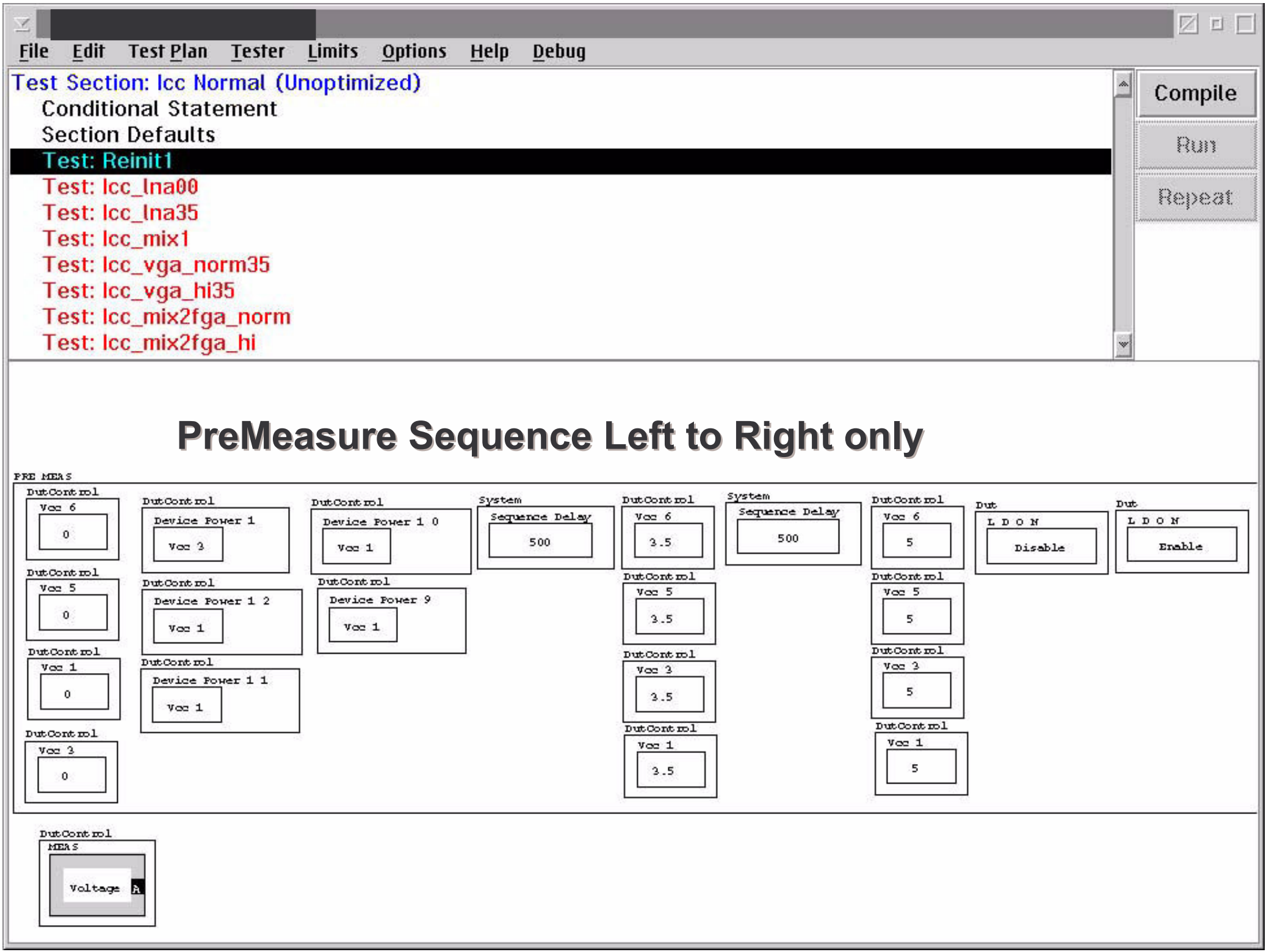
Disconnect Settings Only



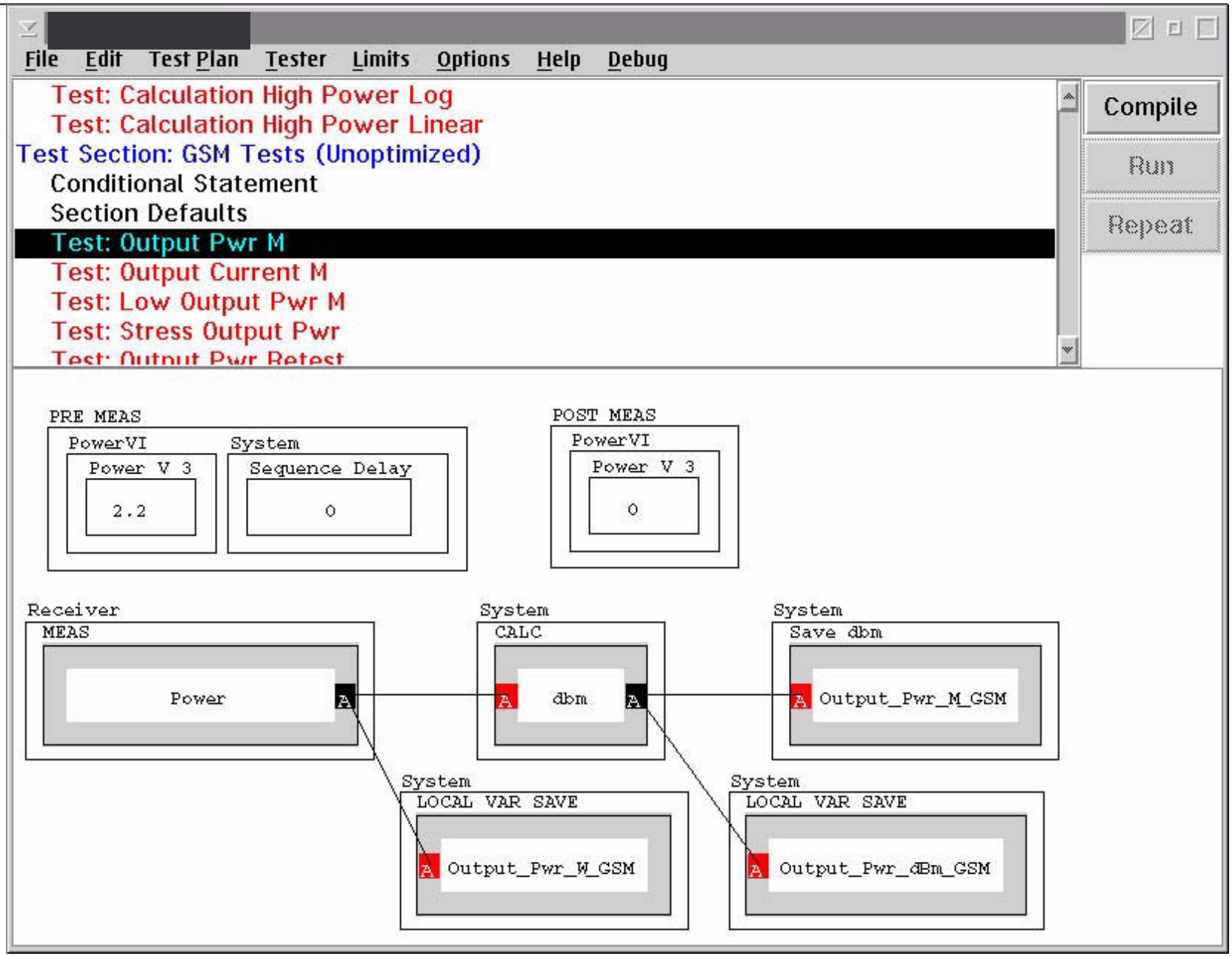
Disconnect Settings Panel
Must include all Parameters set by Local Variable in Test Plan

Connect Sequence: Left to Right only

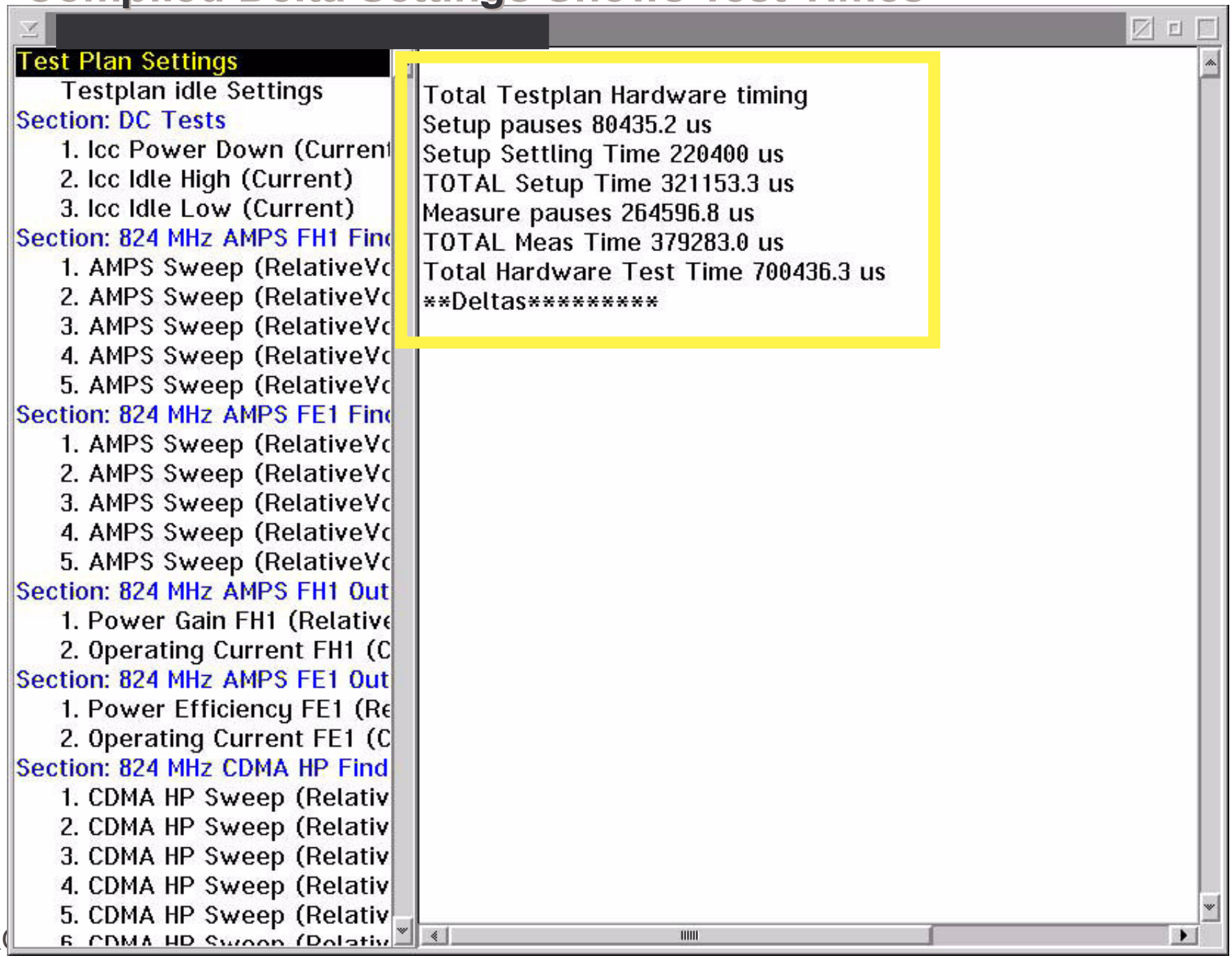



File Edit Test Plan Tester Limits Options Help Debug
Test Section: Icc Normal (Unoptimized)
Conditional Statement
Section Defaults
Test: Reinit1
Test: Icc_lna00
Test: Icc_lna35
Test: Icc_mix1
Test: Icc_vga_norm35
Test: Icc_vga_hi35
Test: Icc_mix2fga_norm
Test: Icc_mix2fga_hi
Compile
Run
Repeat
PreMeasure Sequence Left to Right only
PRE MEAS
DutControl
Vcc 6
0
DutControl
Vcc 5
0
DutControl
Vcc 1
0
DutControl
Vcc 3
0
DutControl
Device Power 1
Vcc 3
DutControl
Device Power 1 2
Vcc 1
DutControl
Device Power 1 1
Vcc 1
DutControl
Device Power 1 0
Vcc 1
DutControl
Device Power 9
Vcc 1
System
Sequence Delay
500
DutControl
Vcc 6
3.5
DutControl
Vcc 5
3.5
DutControl
Vcc 3
3.5
DutControl
Vcc 1
3.5
System
Sequence Delay
500
DutControl
Vcc 6
5
DutControl
Vcc 5
5
DutControl
Vcc 3
5
DutControl
Vcc 1
5
Dut
L D O N
Disable
Dut
L D O N
Enable
DutControl
MEAS
Voltage

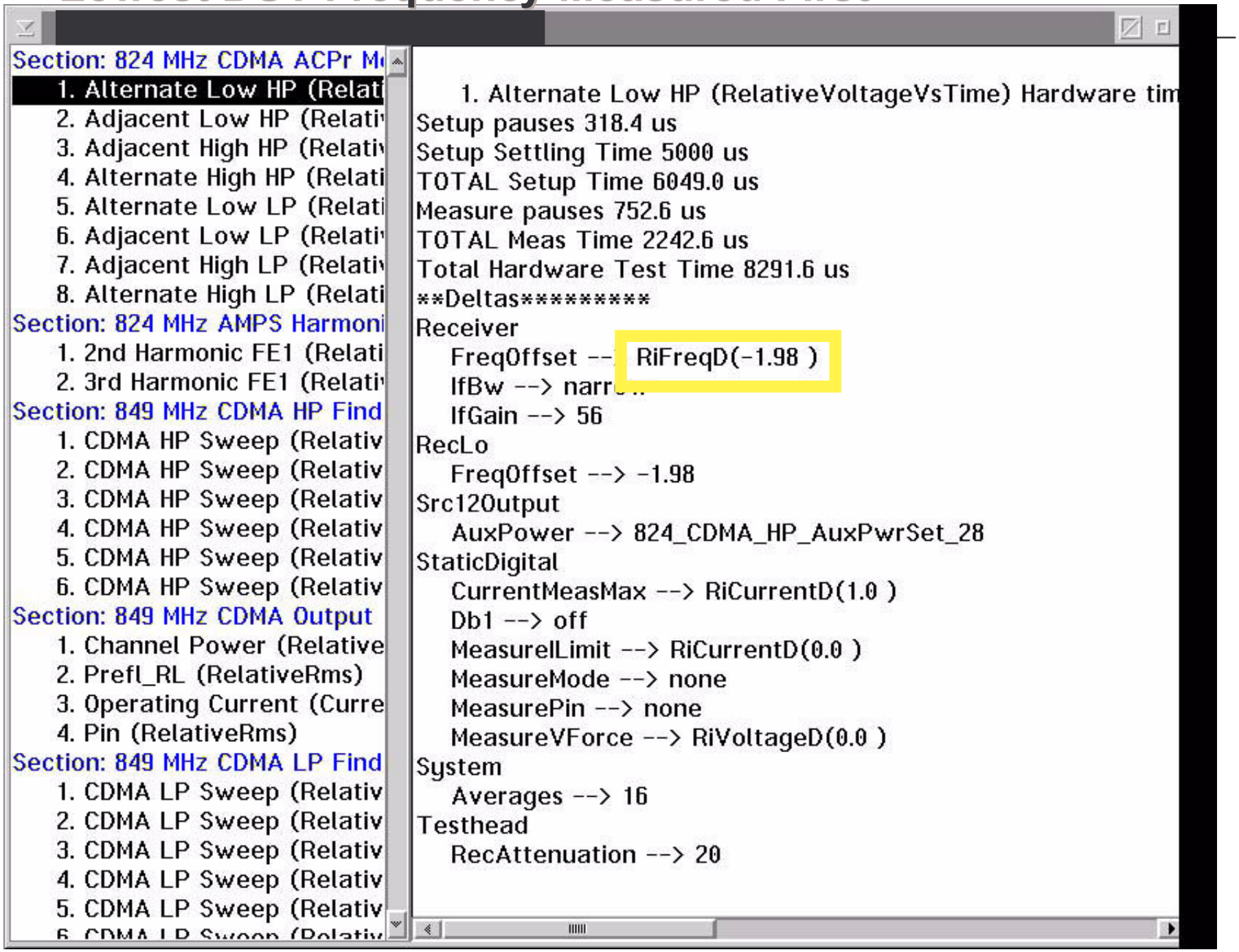
GSM Pulse Sequence, Pulse Voltage and Measure Power Using Pre Measure and Post Measure Groups



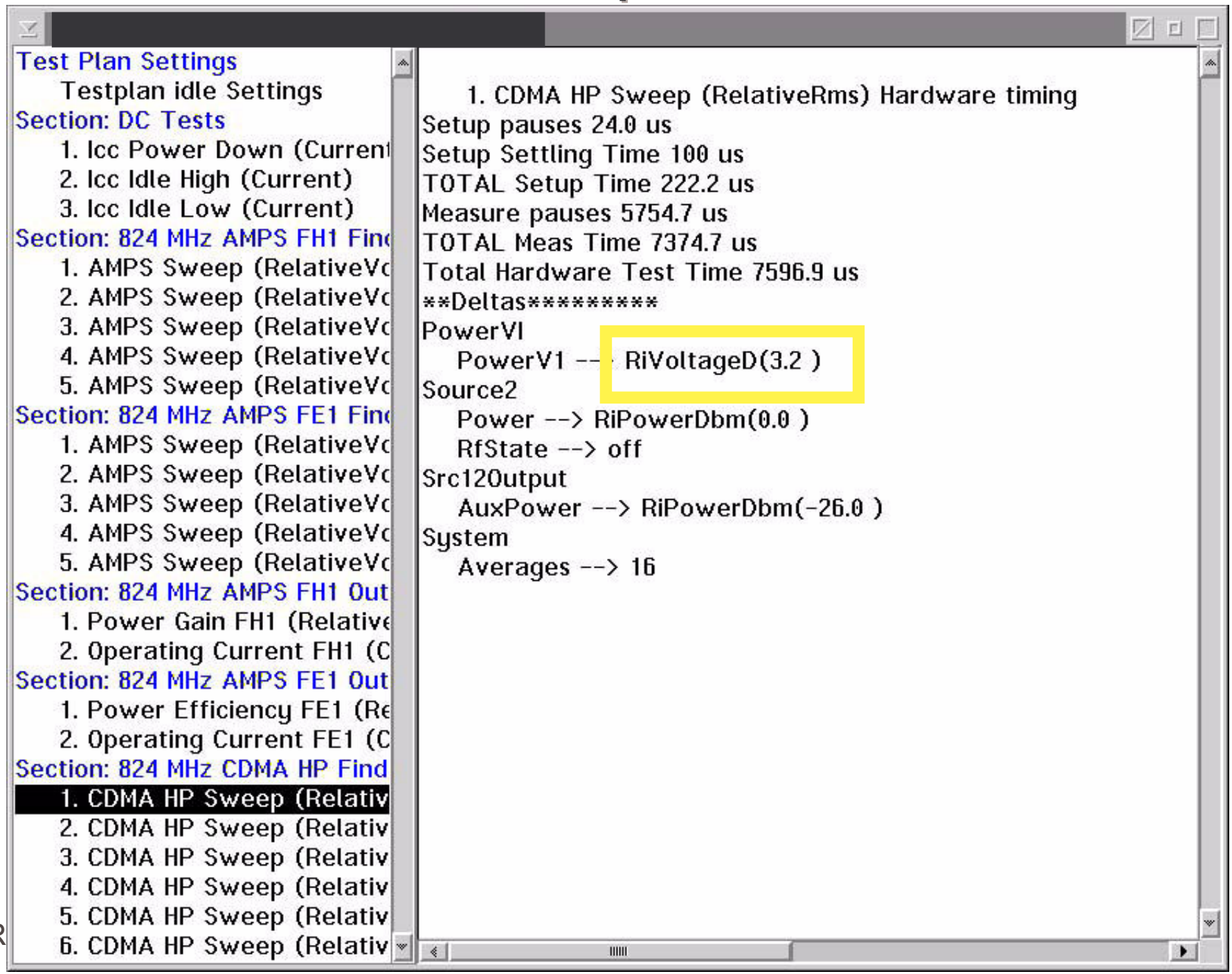
Optimizer: Optimizes over each Test Section. Compiled Delta Settings Shows Test Times



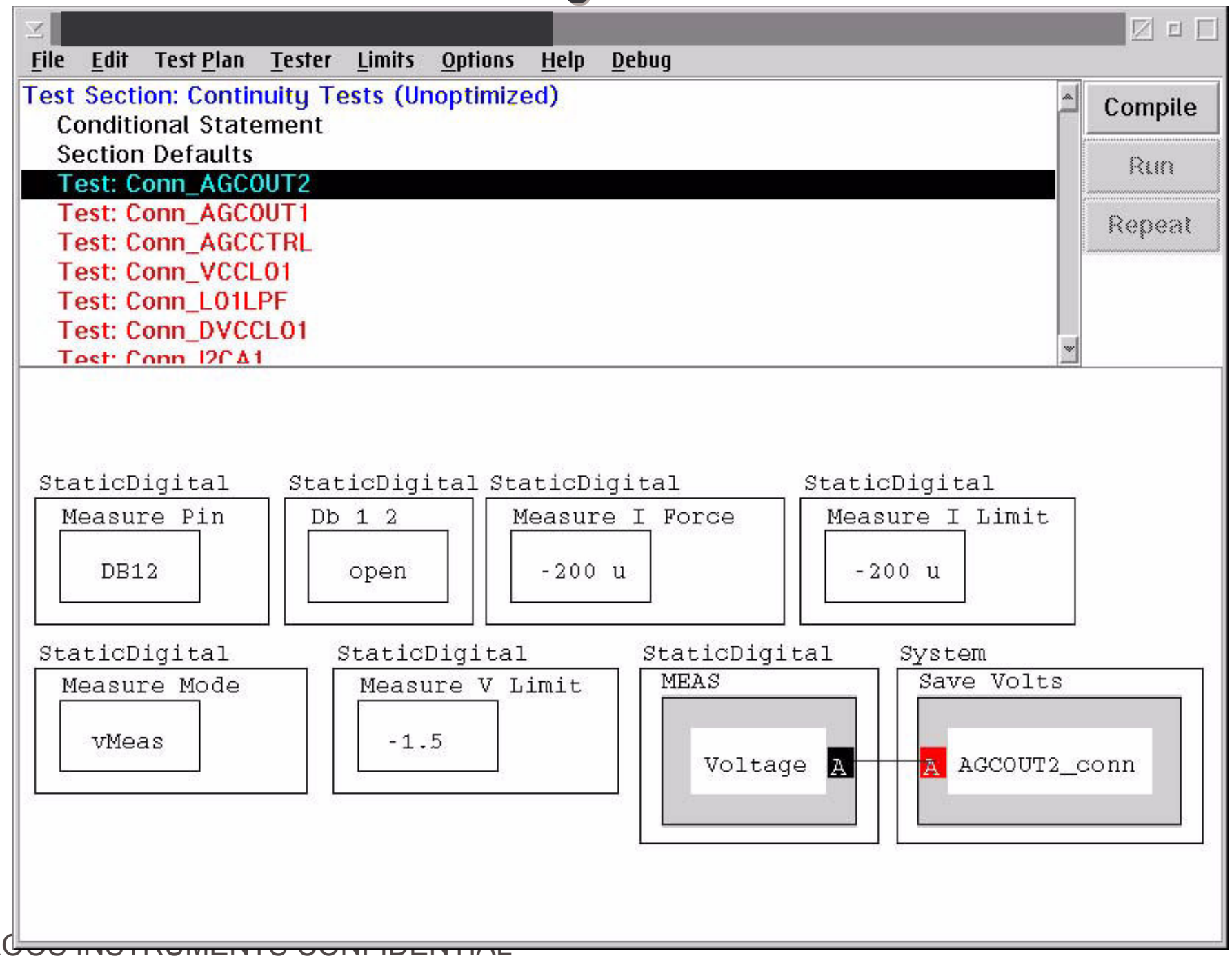
Optimizer: Optimizes each Test Section. Lowest DUT Frequency Measured First



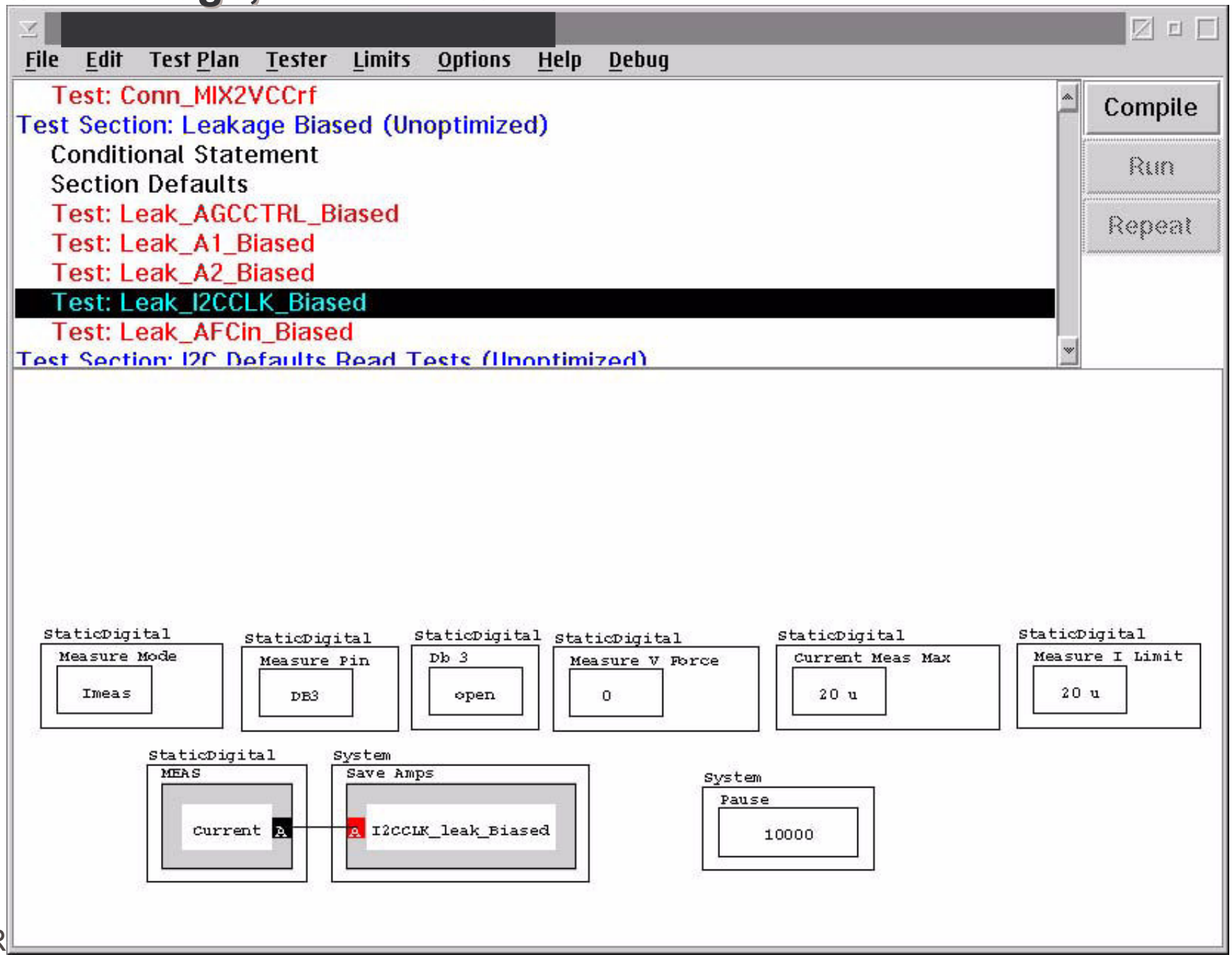
Optimizer: Optimizes each Test Section. Measurement with Lowest Input Power Performed First

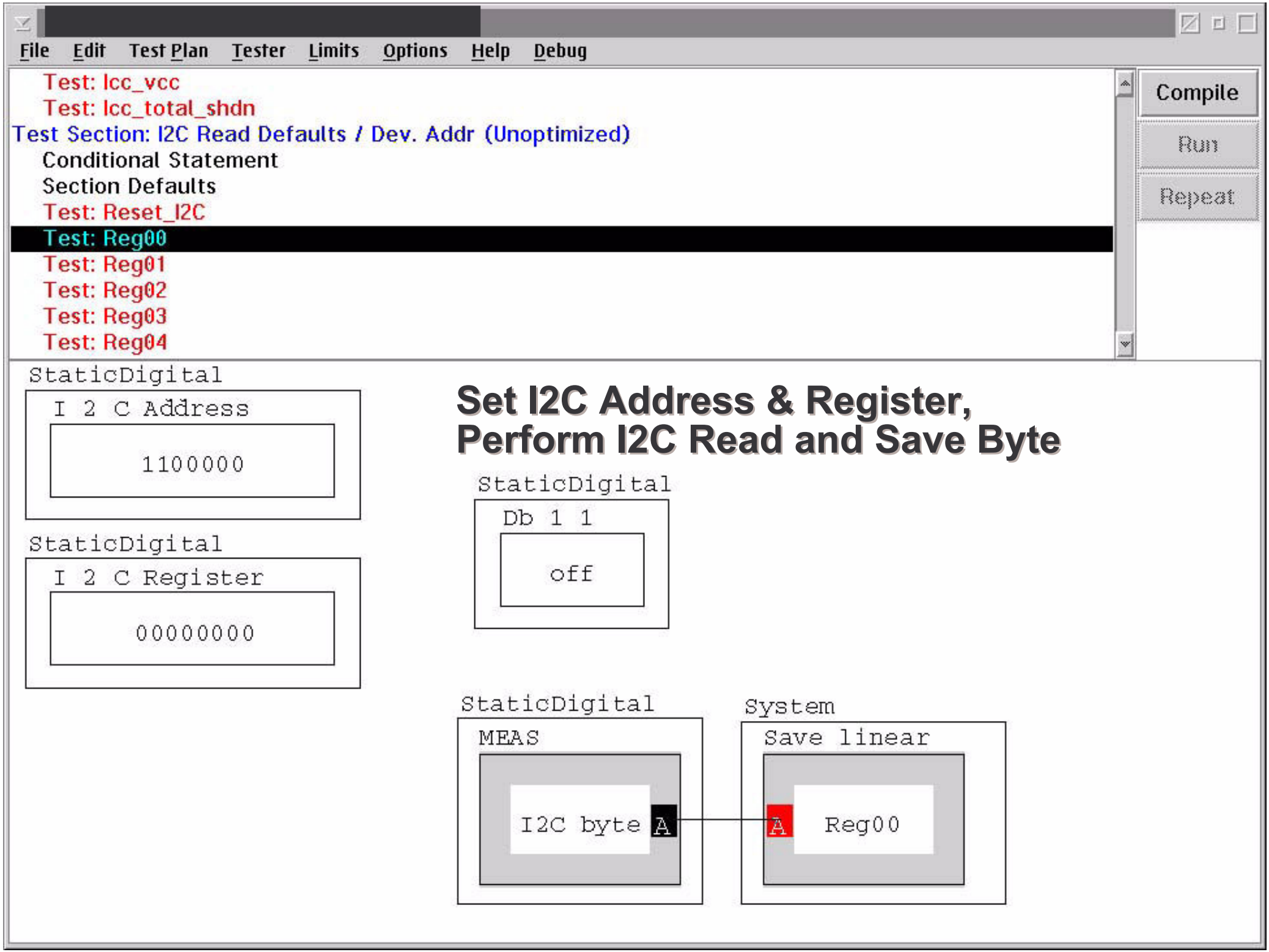


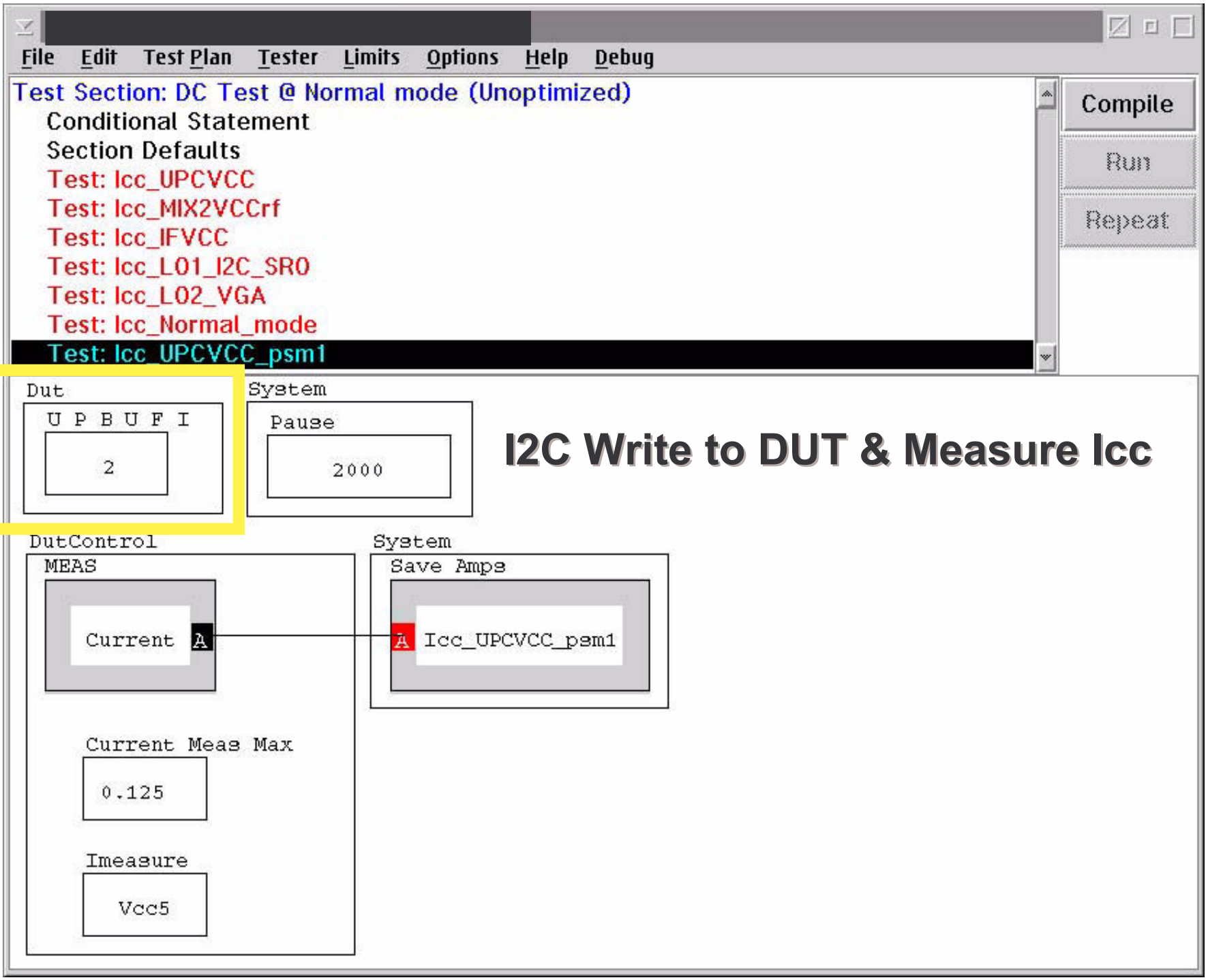
Static Digital Settings for Continuity Test: Set Current Measure Voltage

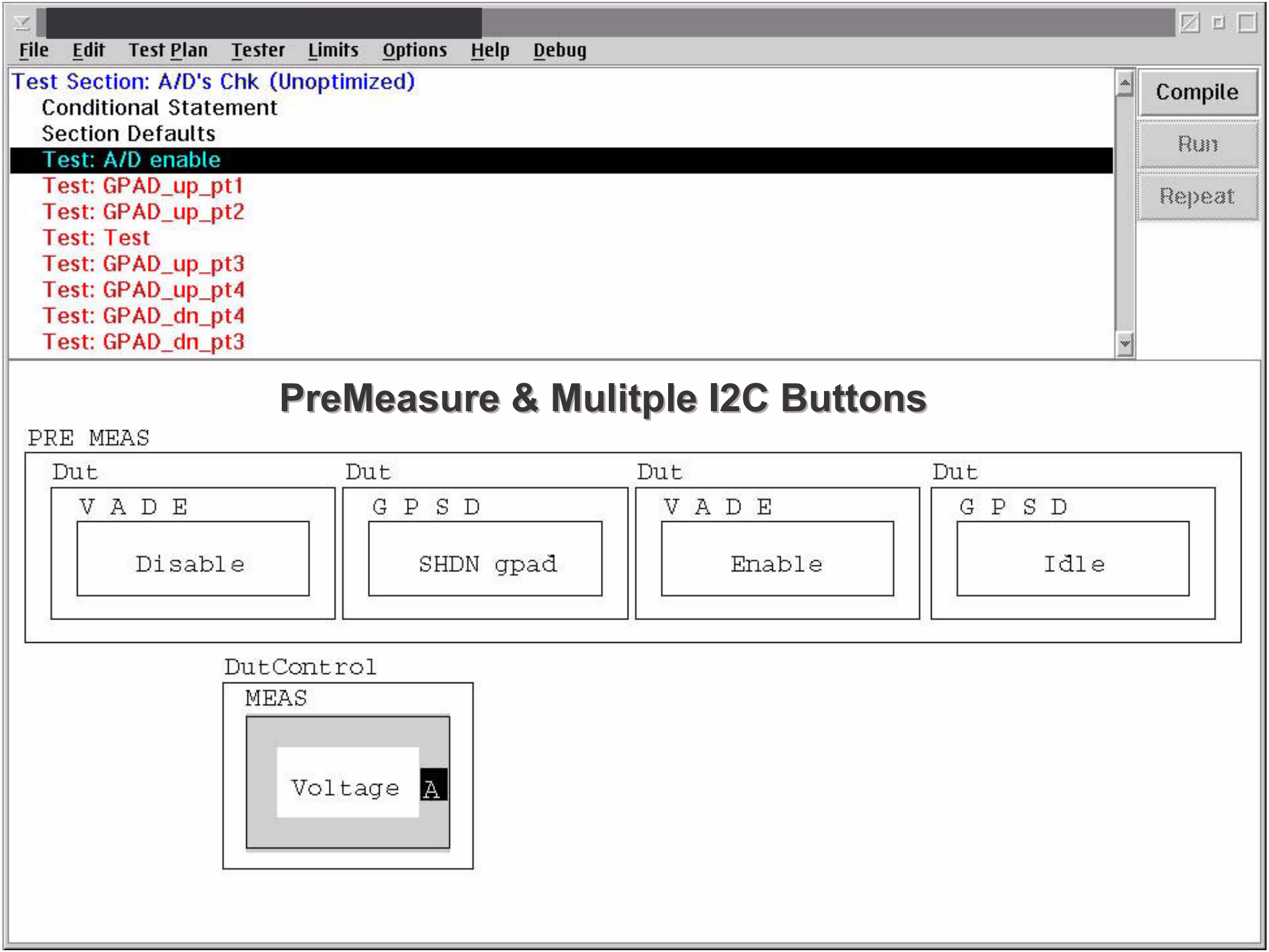


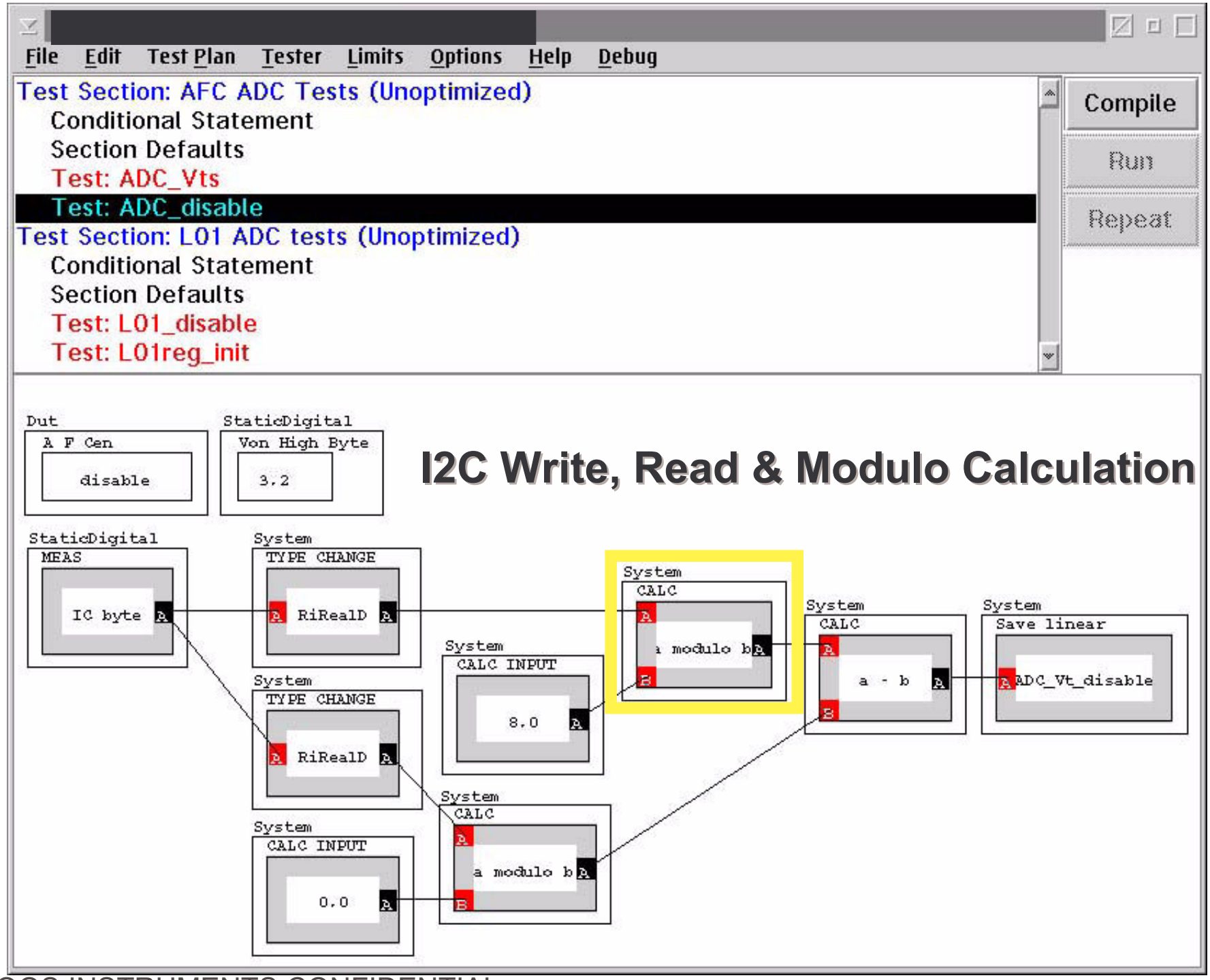
Static Digital Settings for Leakage Test
Set Voltage, Measure Current

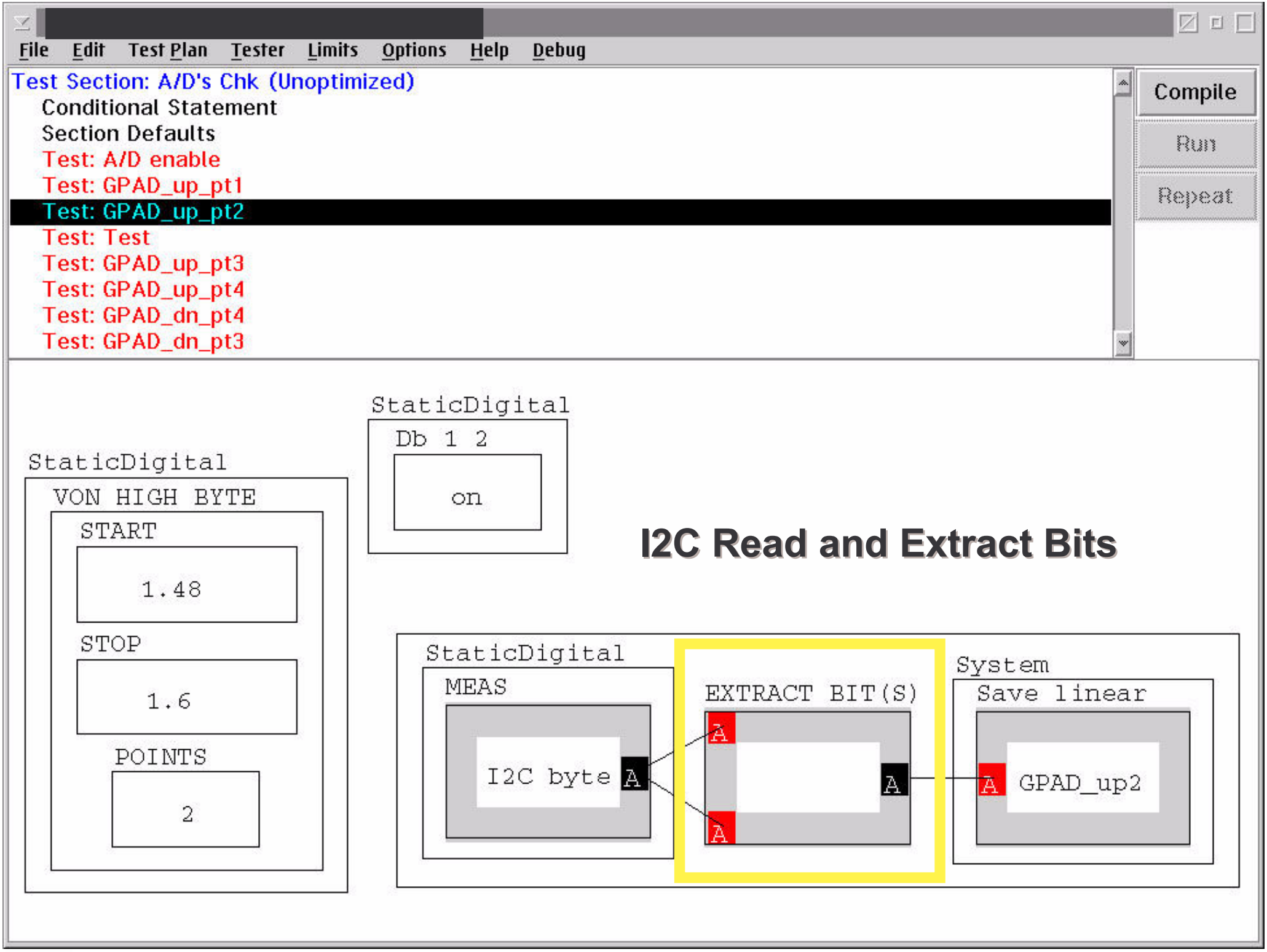



File Edit Test Plan Tester Limits Options Help Debug
Test: Icc_vcc
Test: Icc_total_shdn
Test Section: I2C Read Defaults / Dev. Addr (Unoptimized)
Conditional Statement
Section Defaults
Test: Reset_I2C
Test: Reg00
Test: Reg01
Test: Reg02
Test: Reg03
Test: Reg04
Compile
Run
Repeat
StaticDigital
I 2 C Address
1100000
StaticDigital
I 2 C Register
00000000
Set I2C Address & Register,
Perform I2C Read and Save Byte
StaticDigital
Db 1 1
off
StaticDigital
MEAS
I2C byte A
System
Save linear
A
Reg00


File Edit Test Plan Tester Limits Options Help Debug
Test Section: DC Test @ Normal mode (Unoptimized)
Conditional Statement
Section Defaults
Test: Icc_UPCVCC
Test: Icc_MIX2VCCrf
Test: Icc_IFVCC
Test: Icc_LO1_I2C_SRO
Test: Icc_LO2_VGA
Test: Icc_Normal_mode
Test: Icc_UPCVCC_psm1
Compile
Run
Repeat
Dut
U P B U F I
2
System
Pause
2000
I2C Write to DUT & Measure Icc
DutControl
MEAS
Current A
Current Meas Max
0.125
Imeasure
Vcc5
System
Save Amps
A Icc_UPCVCC_psm1


File Edit Test Plan Tester Limits Options Help Debug
Test Section: A/D's Chk (Unoptimized)
Conditional Statement
Section Defaults
Test: A/D enable
Test: GPAD_up_pt1
Test: GPAD_up_pt2
Test: Test
Test: GPAD_up_pt3
Test: GPAD_up_pt4
Test: GPAD_dn_pt4
Test: GPAD_dn_pt3
Compile
Run
Repeat
PreMeasure & Mulitple I2C Buttons
PRE MEAS
Dut
V A D E
Disable
Dut
G P S D
SHDN gpad
Dut
V A D E
Enable
Dut
G P S D
Idle
DutControl
MEAS
Voltage
A



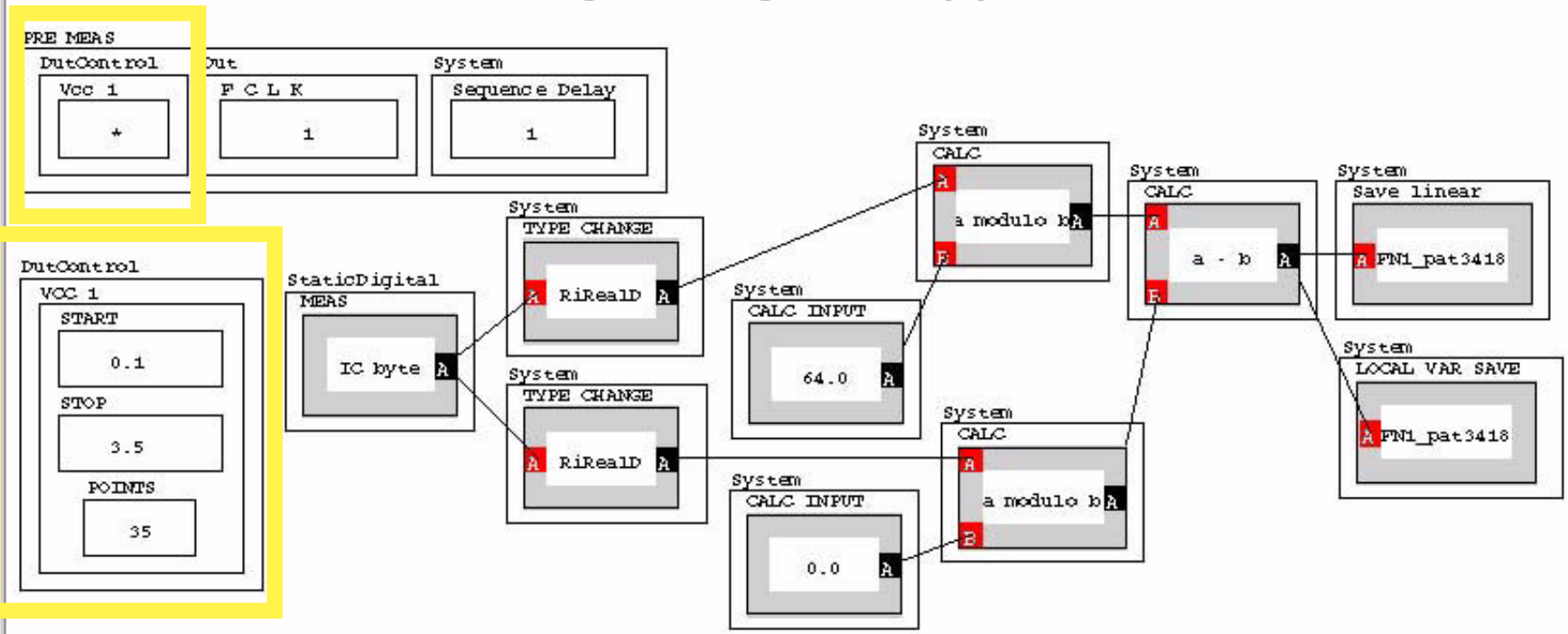

File Edit Test Plan Tester Limits Options Help Debug
Test Section: A/D's Chk (Unoptimized)
Conditional Statement
Section Defaults
Test: A/D enable
Test: GPAD_up_pt1
Test: GPAD_up_pt2
Test: Test
Test: GPAD_up_pt3
Test: GPAD_up_pt4
Test: GPAD_dn_pt4
Test: GPAD_dn_pt3
Compile
Run
Repeat
StaticDigital
Db 1 2
on
StaticDigital
VON HIGH BYTE
START
1.48
STOP
1.6
POINTS
2
I2C Read and Extract Bits
StaticDigital
MEAS
I2C byte
A
EXTRACT BIT(S)
A
A
A
System
Save linear
A
GPAD_up2

File Edit Test Plan Tester Limits Options Help Debug

Test: I2PIND_test@GC15@AGC_3.0V
Test Section: FN1_testmode (Unoptimized)
Conditional Statement
Section Defaults
Test State: FN1_pattern1
Test: FN1_pat3418_init1
Test: FN1_pat3418_init2
Test: FN1_pat3418_init3
Test: CleanFN1_3418
Test: FN1_pat3418

Compile
Run
Repeat

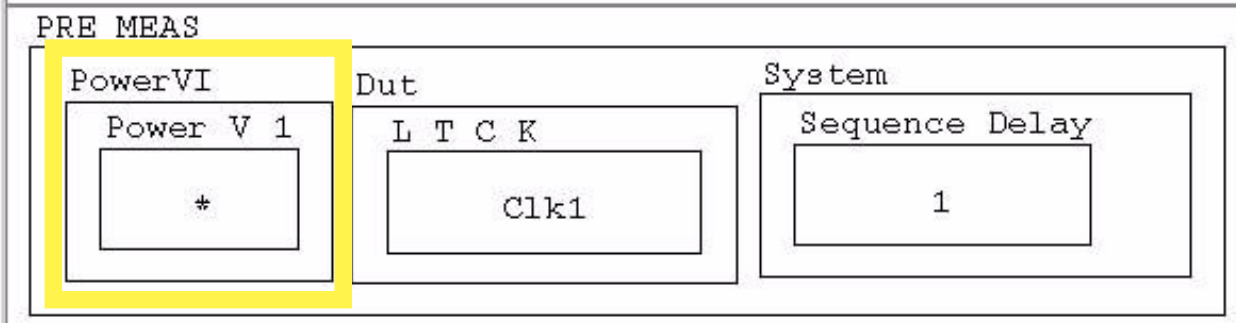
Fractional N Testing Using Vcc1(*)

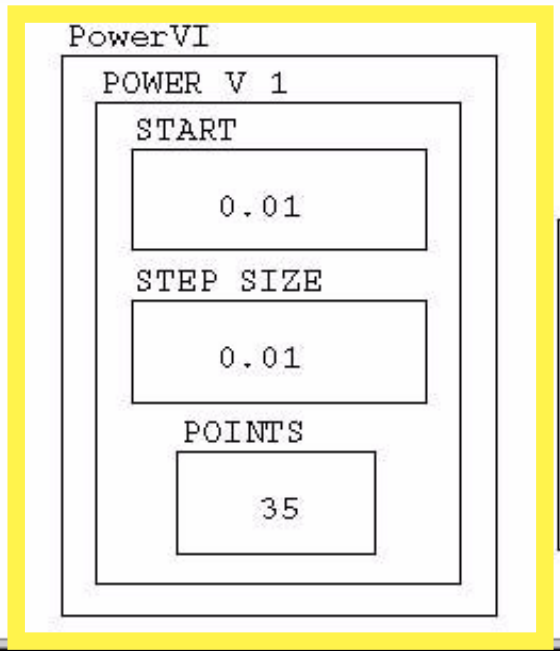


File Edit Test Plan Tester Limits Options Help Debug

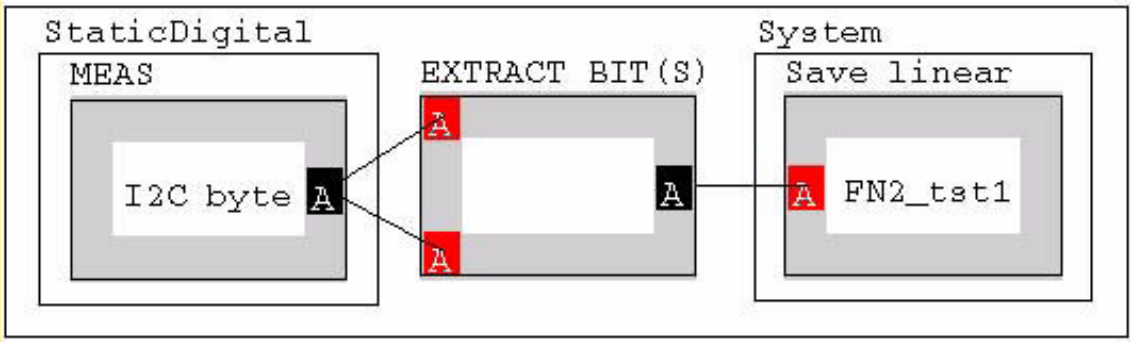
Test Section: FracN testmode (Unoptimized)
Conditional Statement
Section Defaults
Test: FN2 Test init
Test: FN2 Test6836
Test: FN2 Test init1
Test: FN2 Test init2
Test: FN2 Test2020
Test: FN2 Test init1
Test: FN2 Test init2
Test: FN2 Test1354

Compile
Run
Repeat

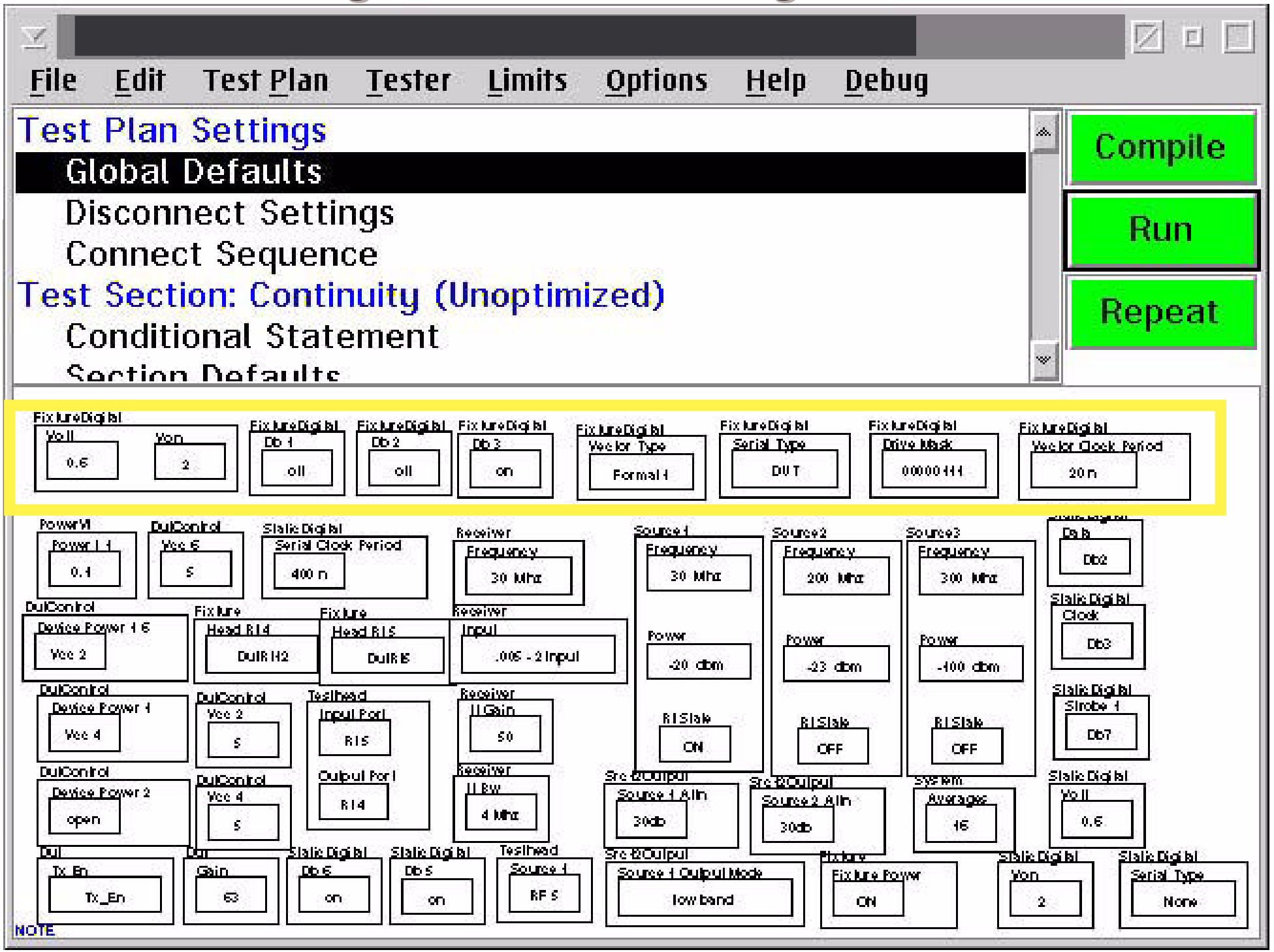




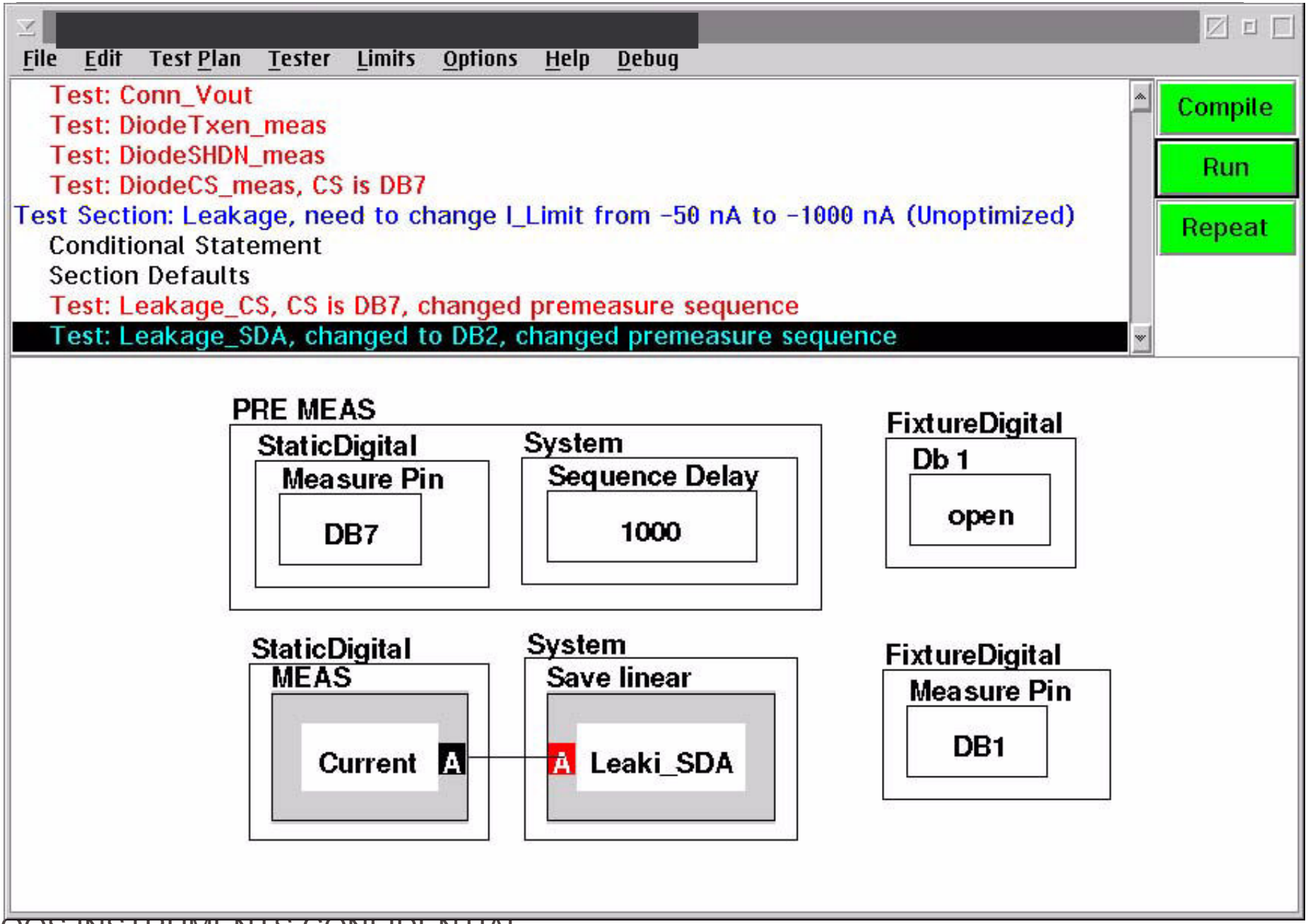
Clocking I2C Bit using VI1(*)



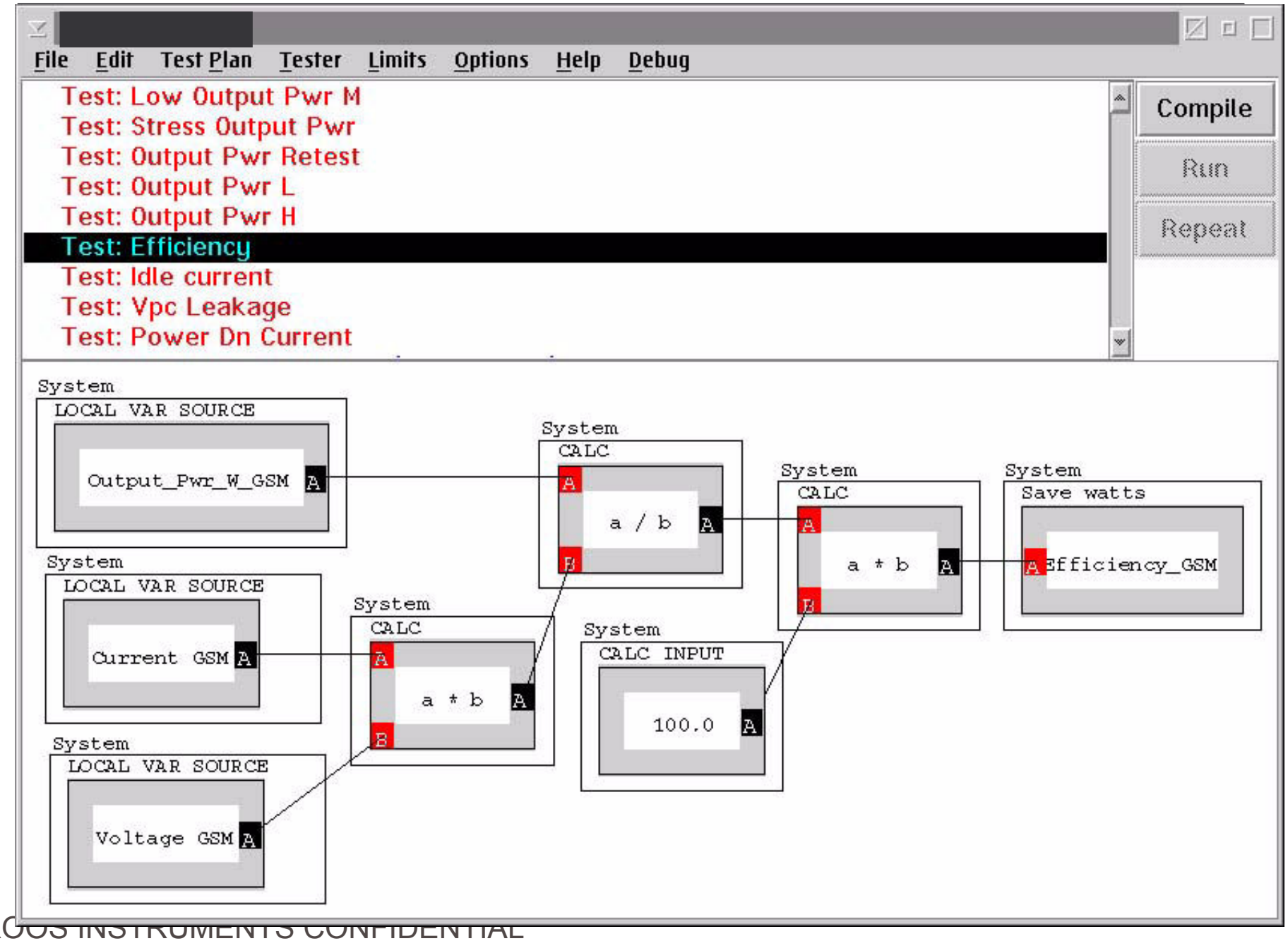
Fixture Digital Default Settings



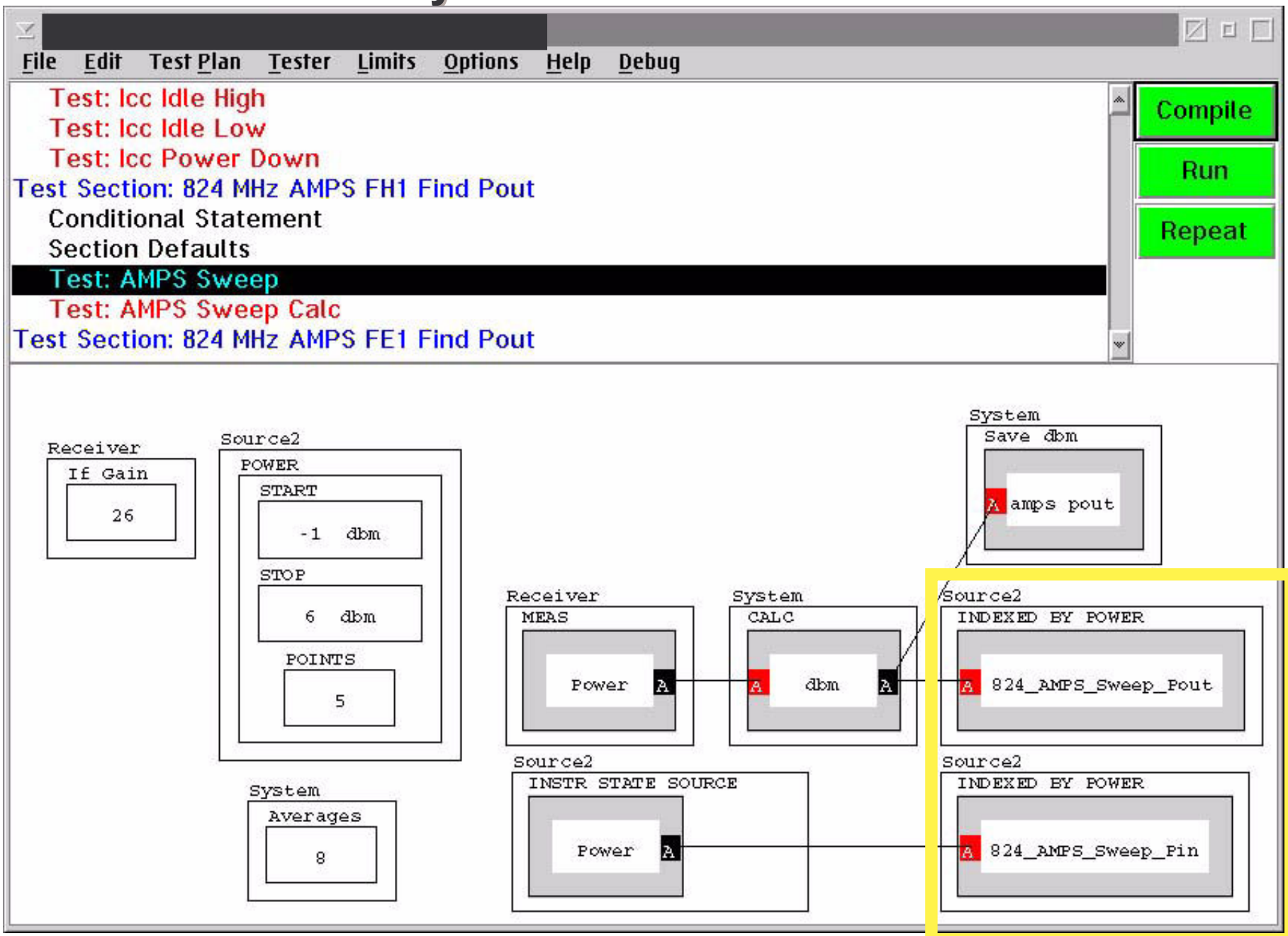
Fixture Digital Leakage Current



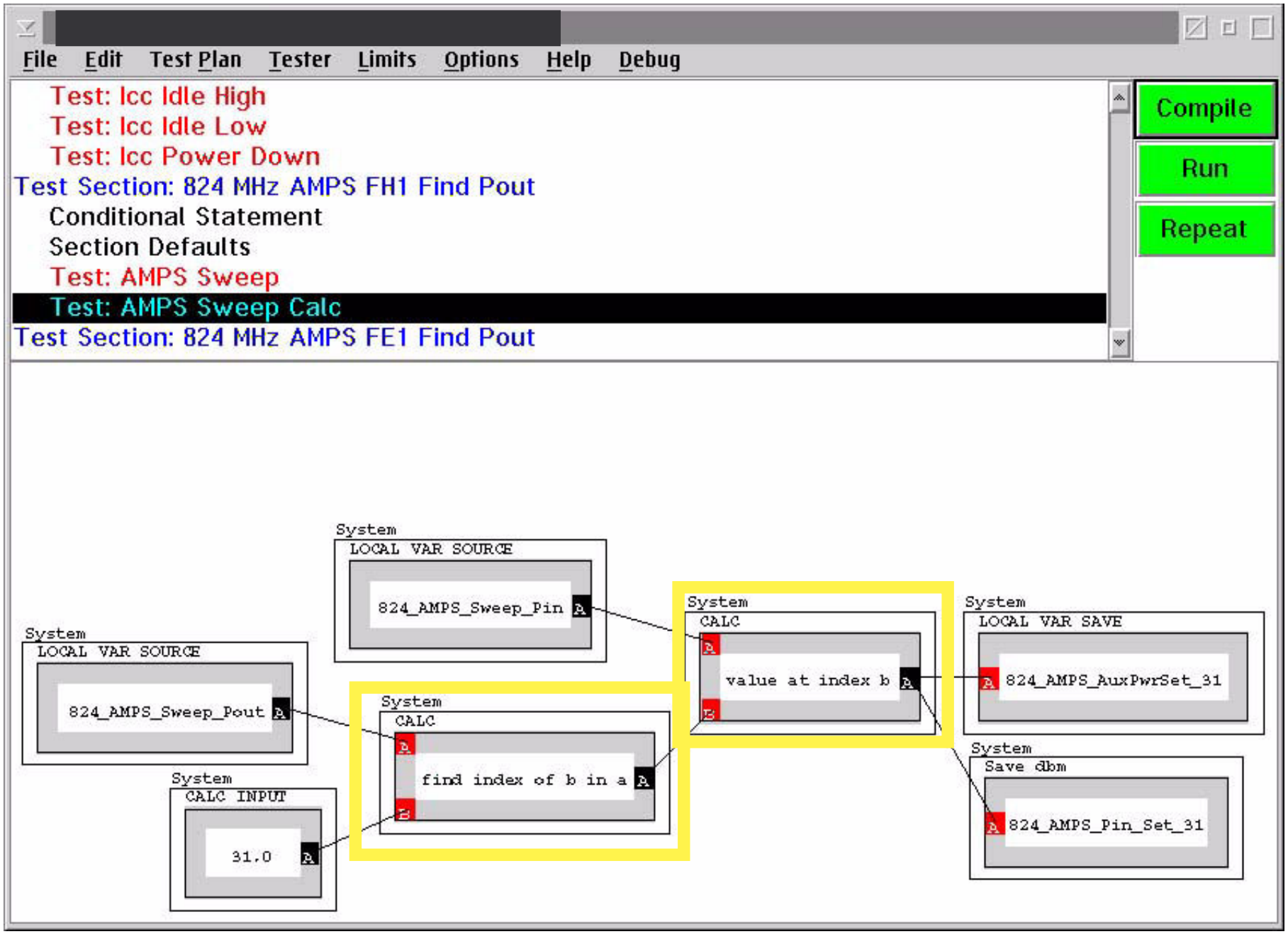
PAE: Power Added Efficiency



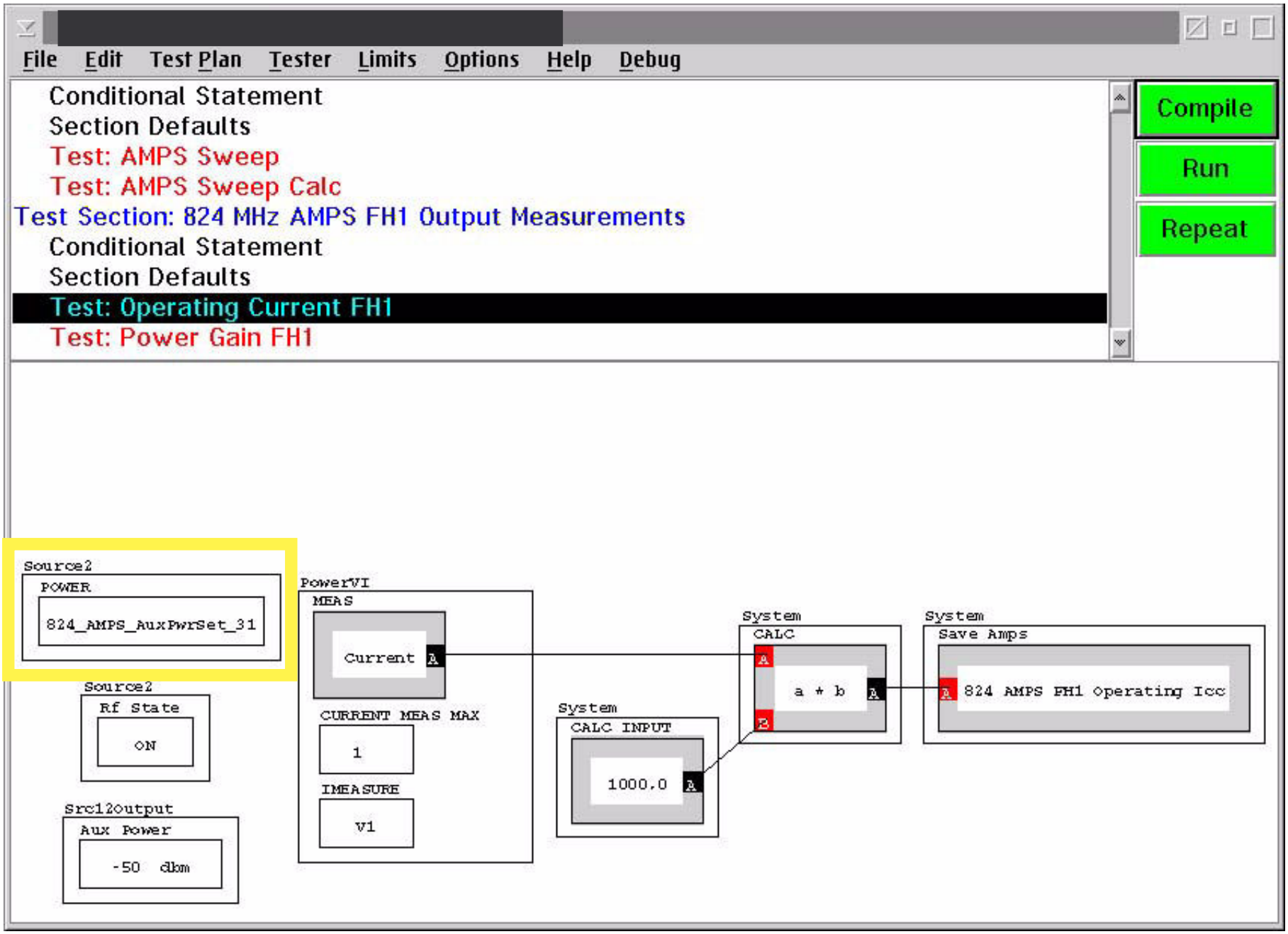
Sweep Pin, Measure Pout, Save Pin and Pout Data in Local Variables indexed by Source 2 Power



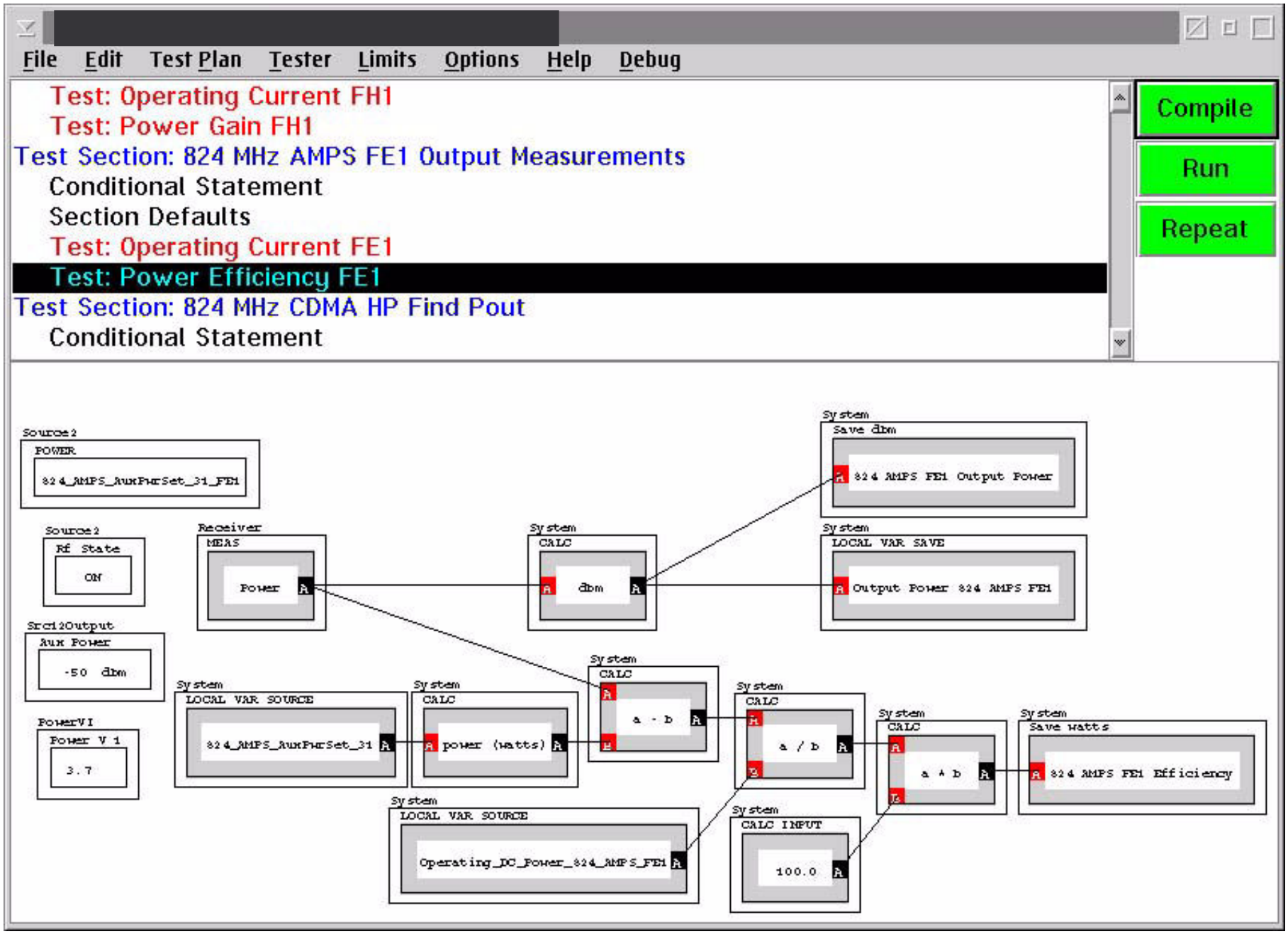
Calculate Pin such that Pout is +31 dBm



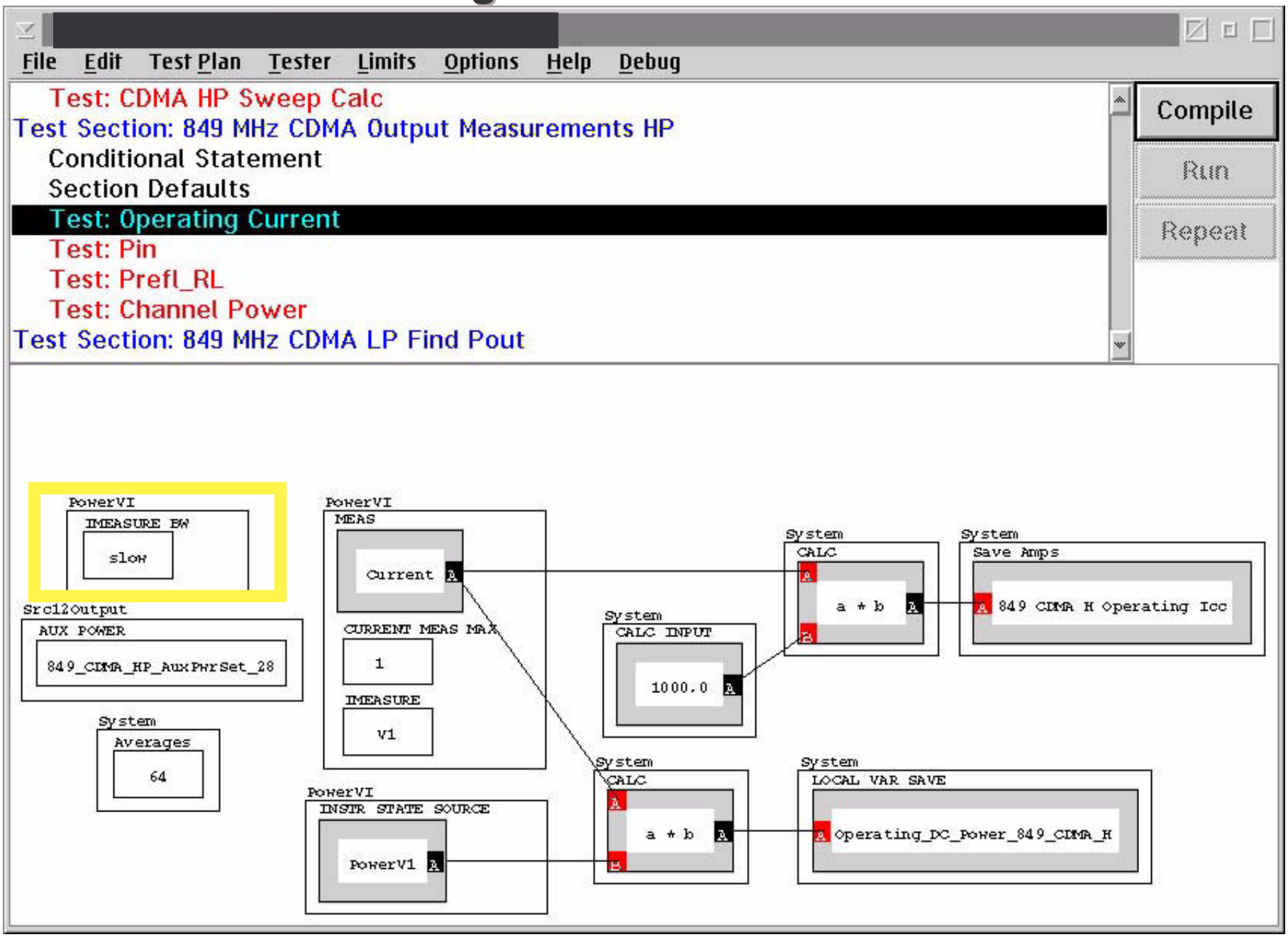
Set Source 2 Input Level using Local Variable, DUT Pout = 31 dBm, Measure Icc



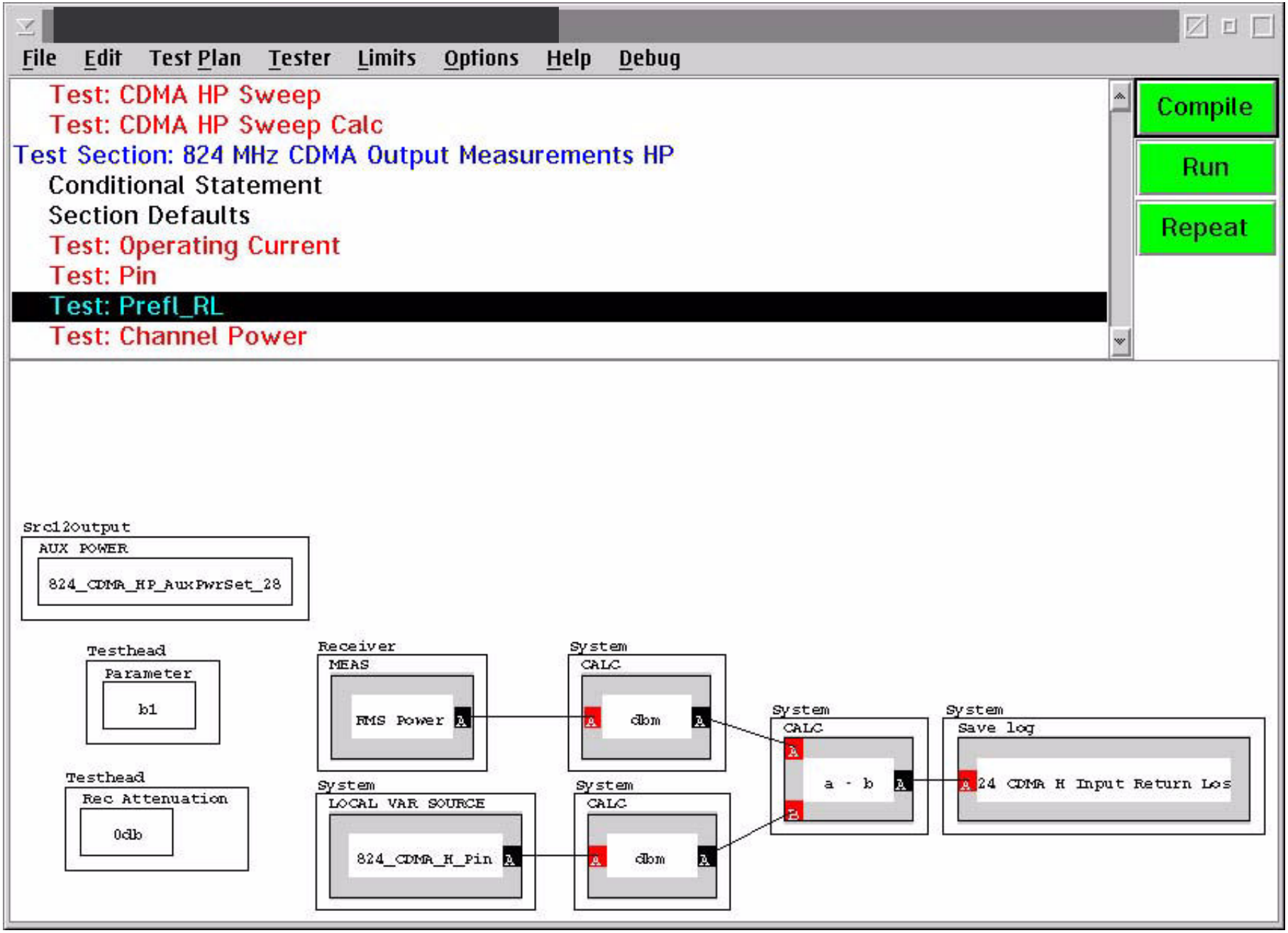
Measure Pout and Calculated PAE for the DUT



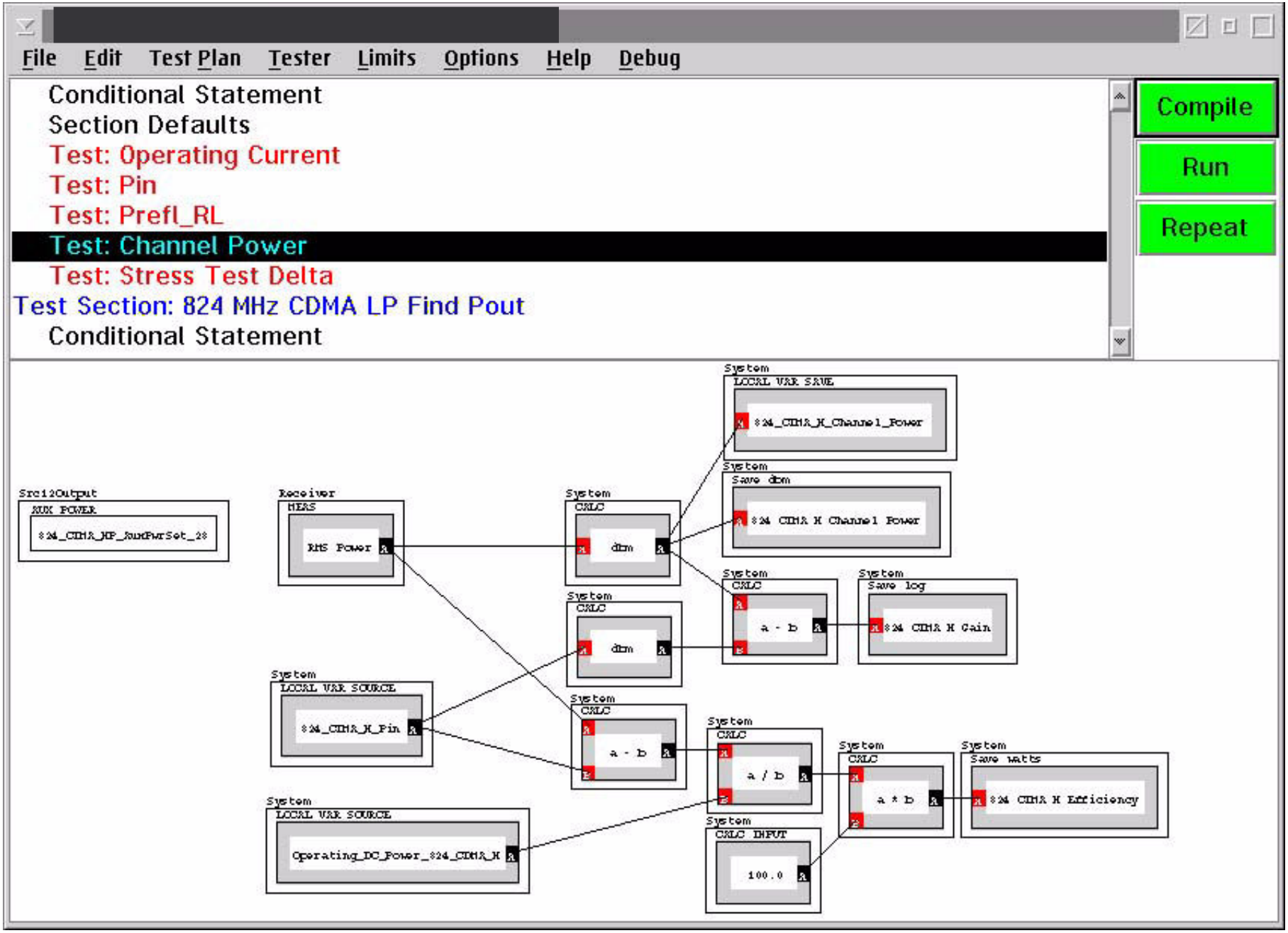
Measure Current using VI1 Imeasure BW set to Slow



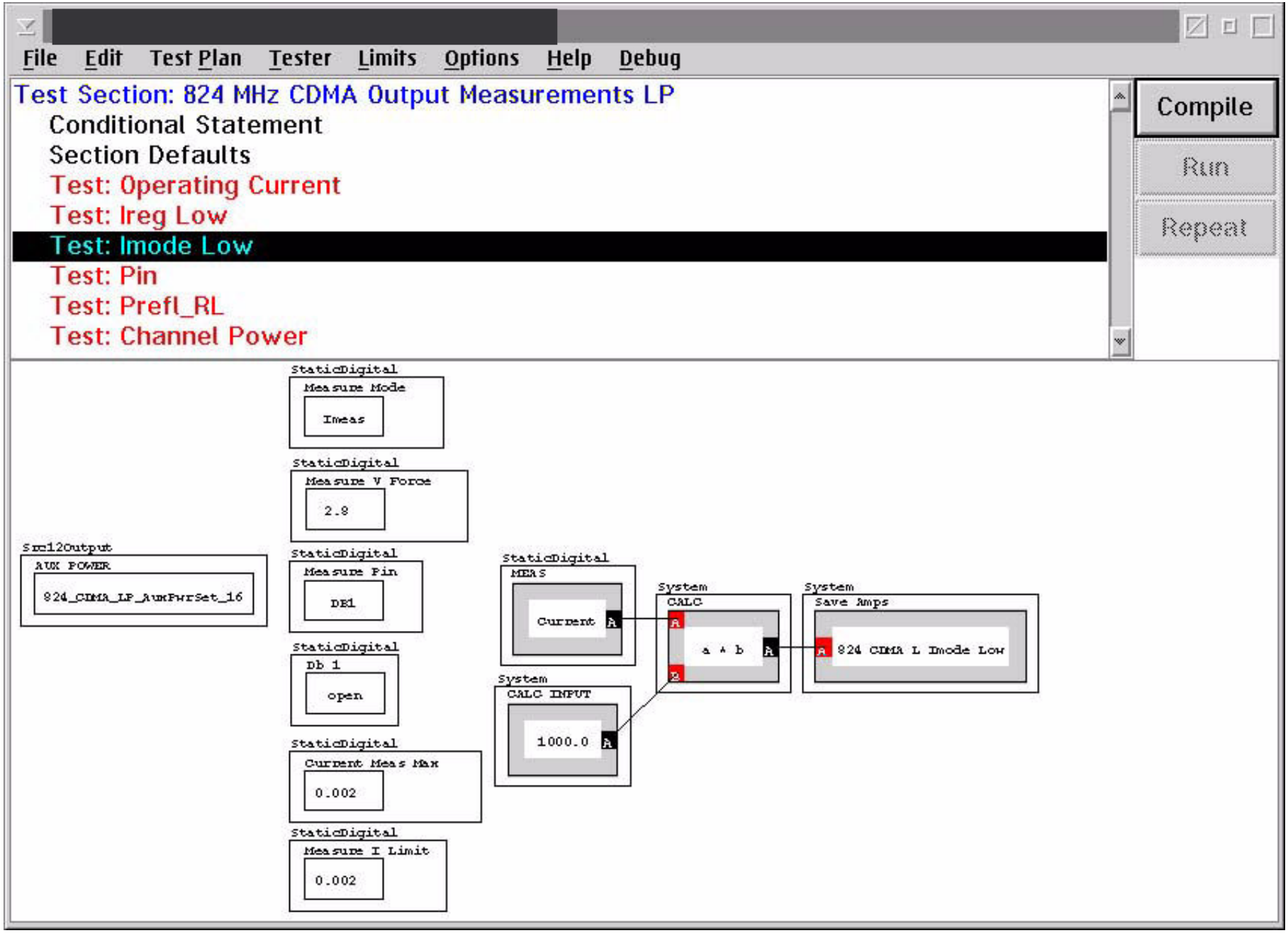
Measure Input Return Loss of a Modulated Signal



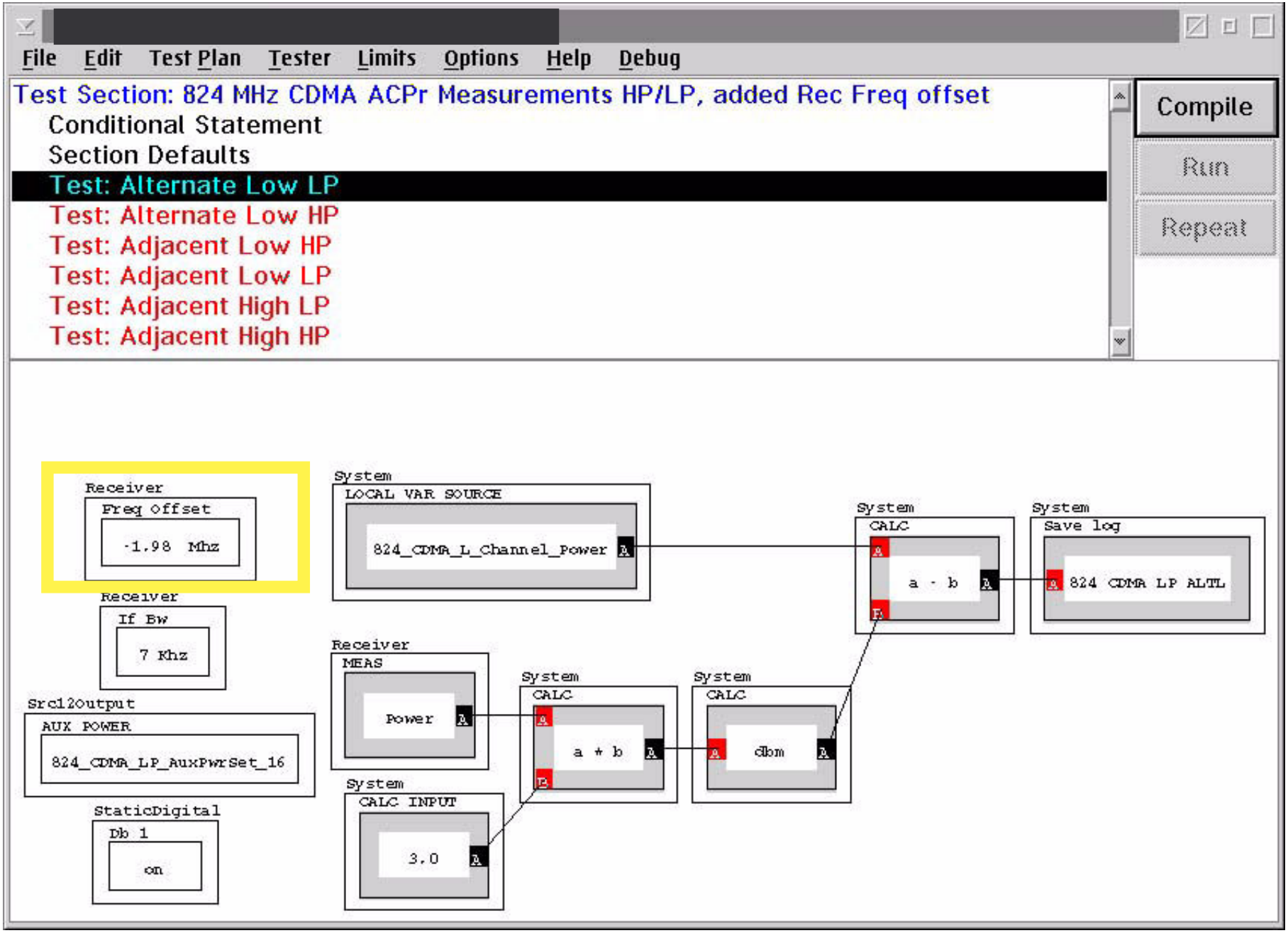
Measure Pout, Calculate Gain & PAE of the DUT with an RF Modulated Signal applied



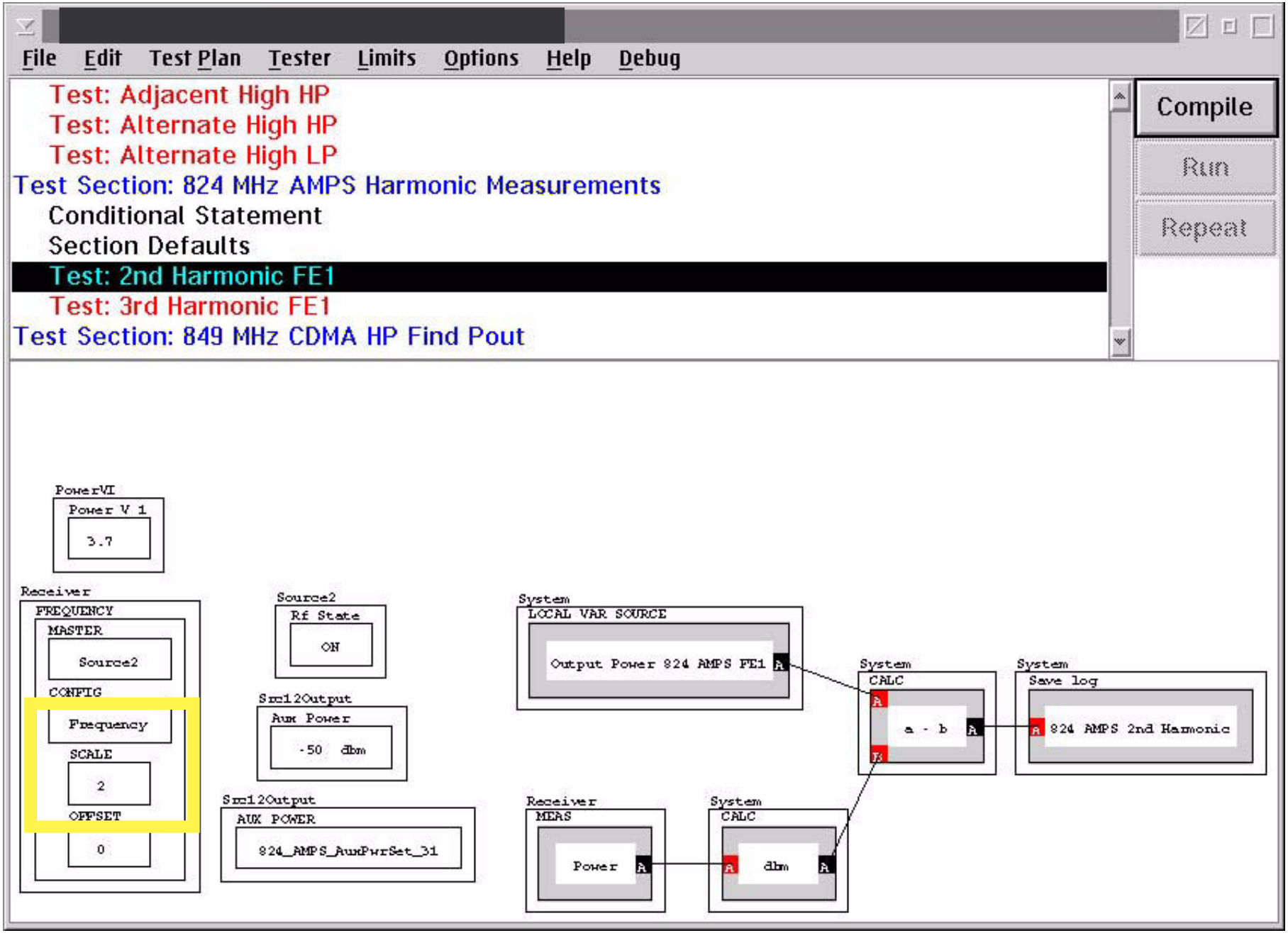
Measure Current using DB 1 Voltage Parametric Capability



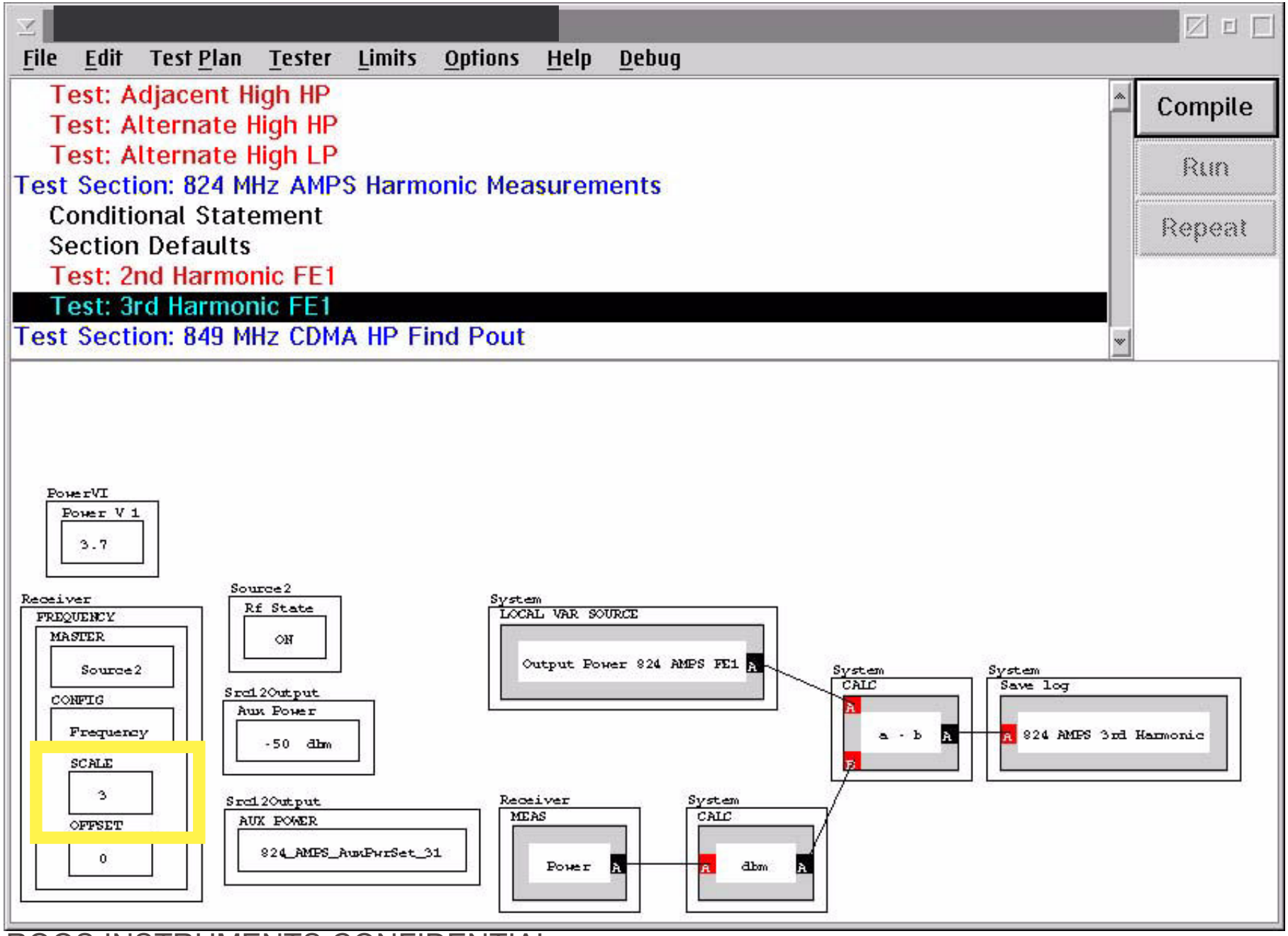
Measure ACPR using Receiver Frequency Offset Button



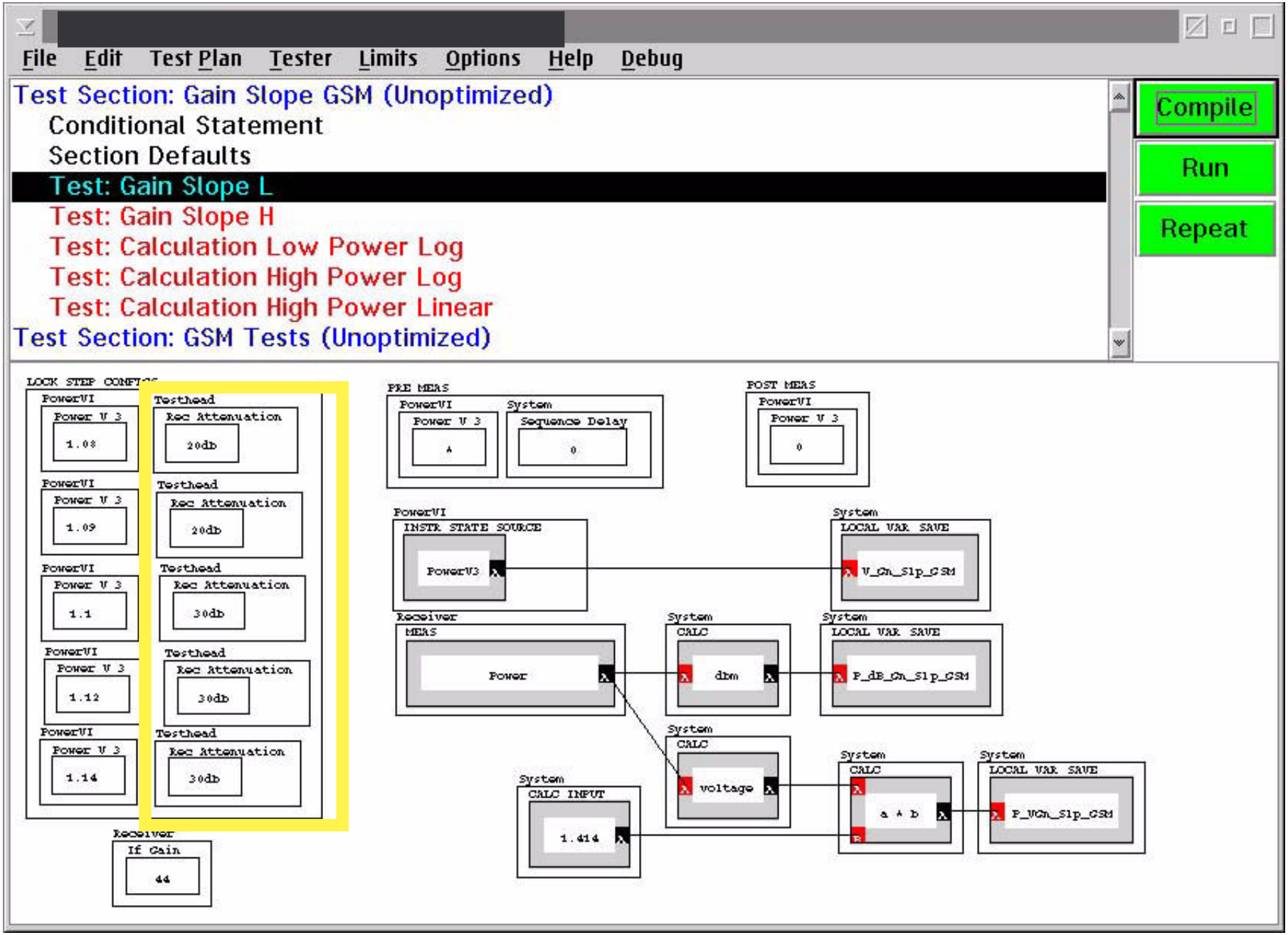
Measure Second Harmonic



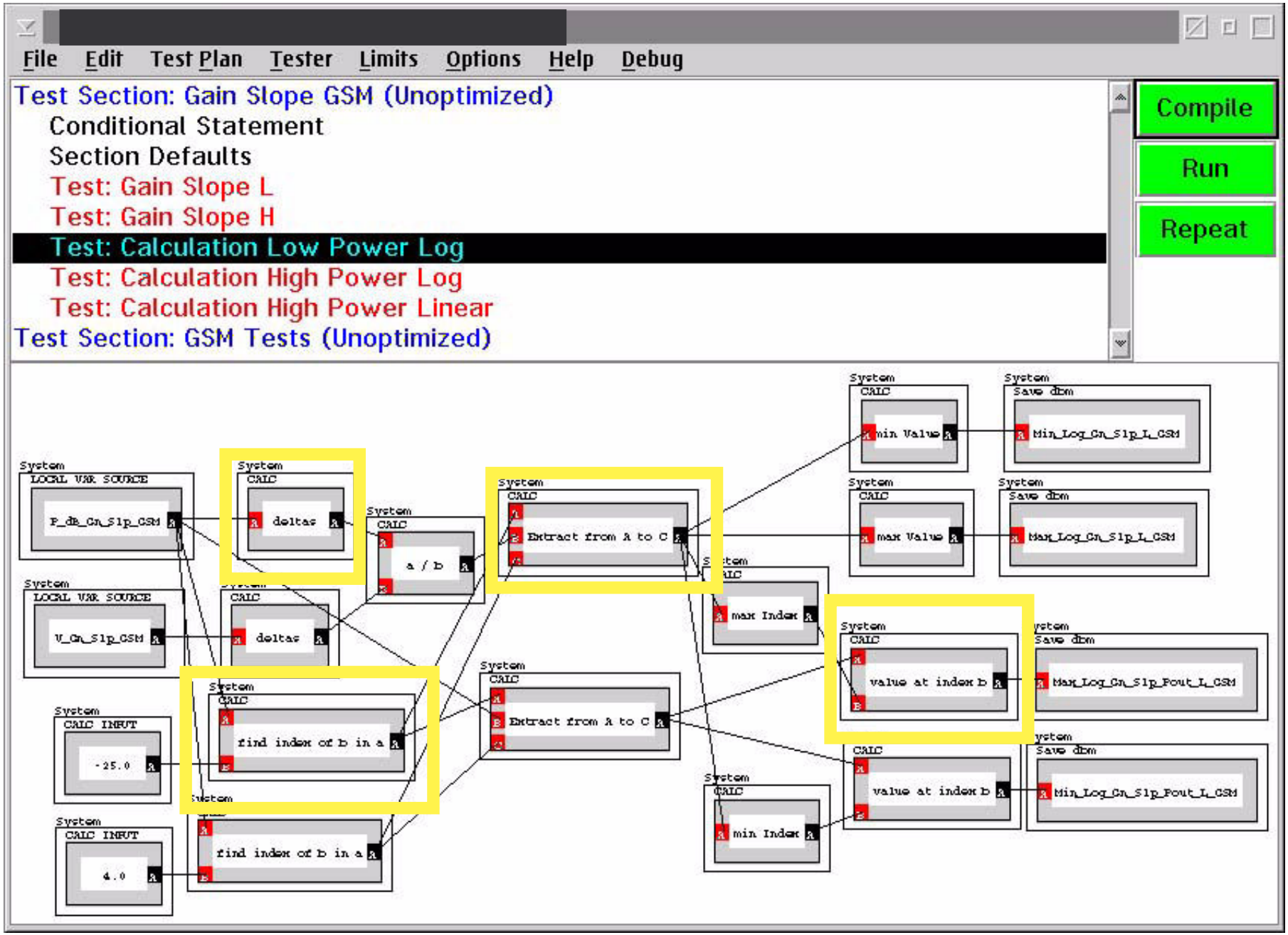
Measure Third Harmonic



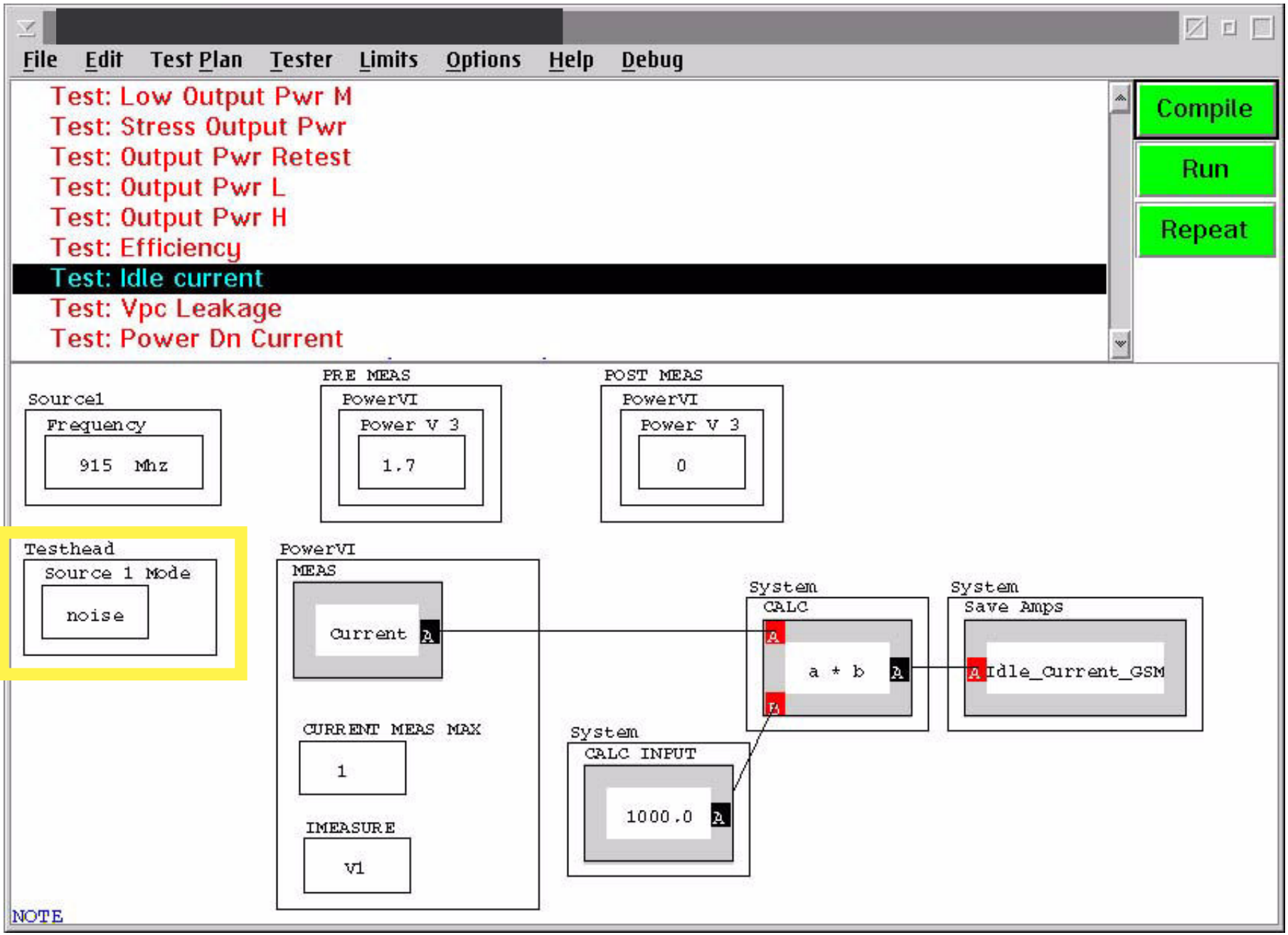
Sweep Power to Find Gain Slope
Use Lock Step to Control Receiver Attenuation



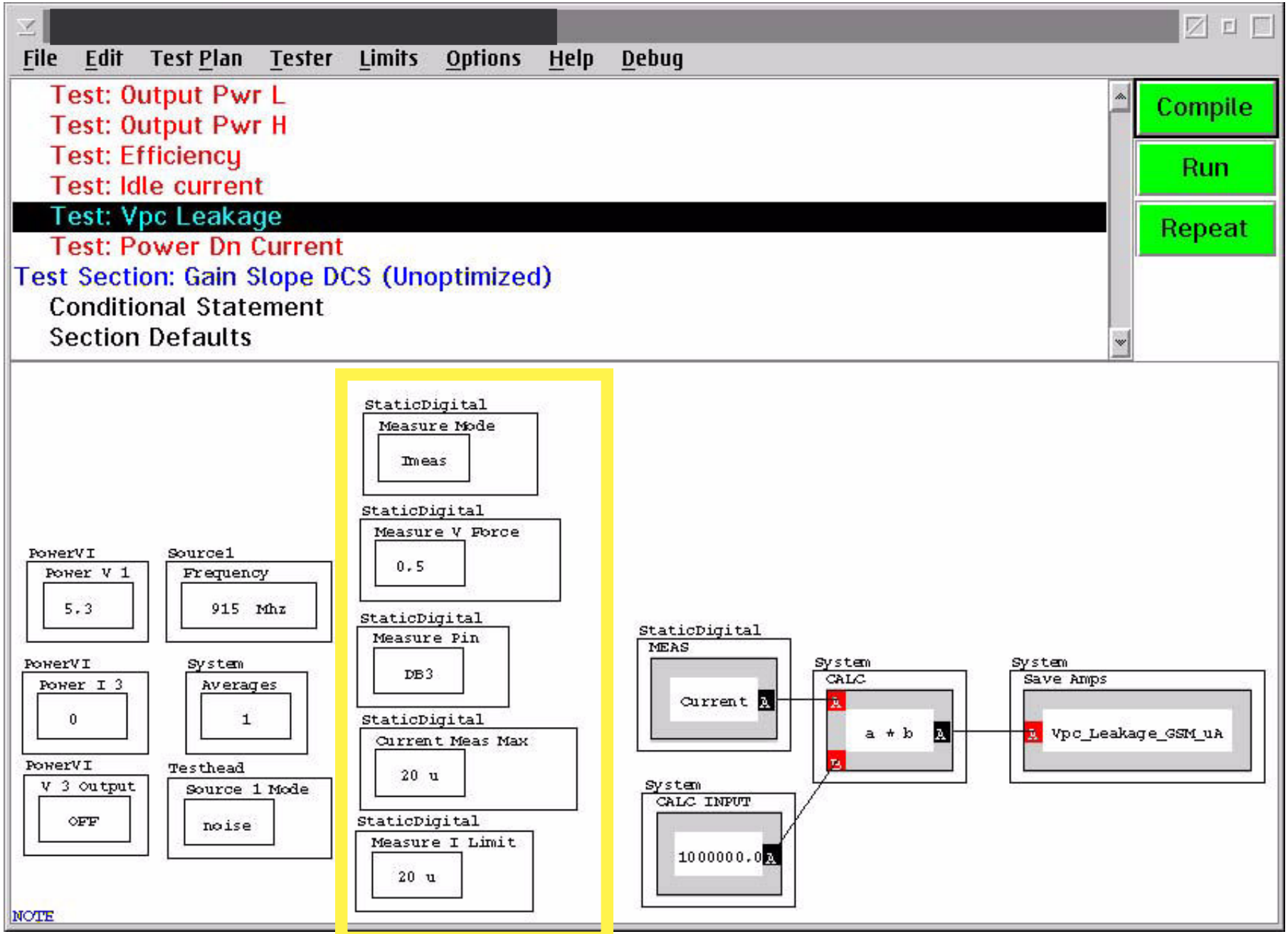
Calc Gain Slope using Deltas, Extract, Find Index & Value at Index



Set Source 1 Mode to Noise: Isolates Source 1 from DUT Measure Pulsed Idle Current



Measure Vpc Pin Leakage Current using DB Line



Measure Power Down Current
Using VI to set Voltage Level & DB to Measure Current