



Controlling the Part

- Static Bits
- Serial and Parallel Interfaces
- Starting up the Part
- Changing States
- Waiting for the Part



DB Lines

- Static digital control
- Serial bus
- Parallel bus
- Leakage (low current) measurements
- ESD diode check (force current)



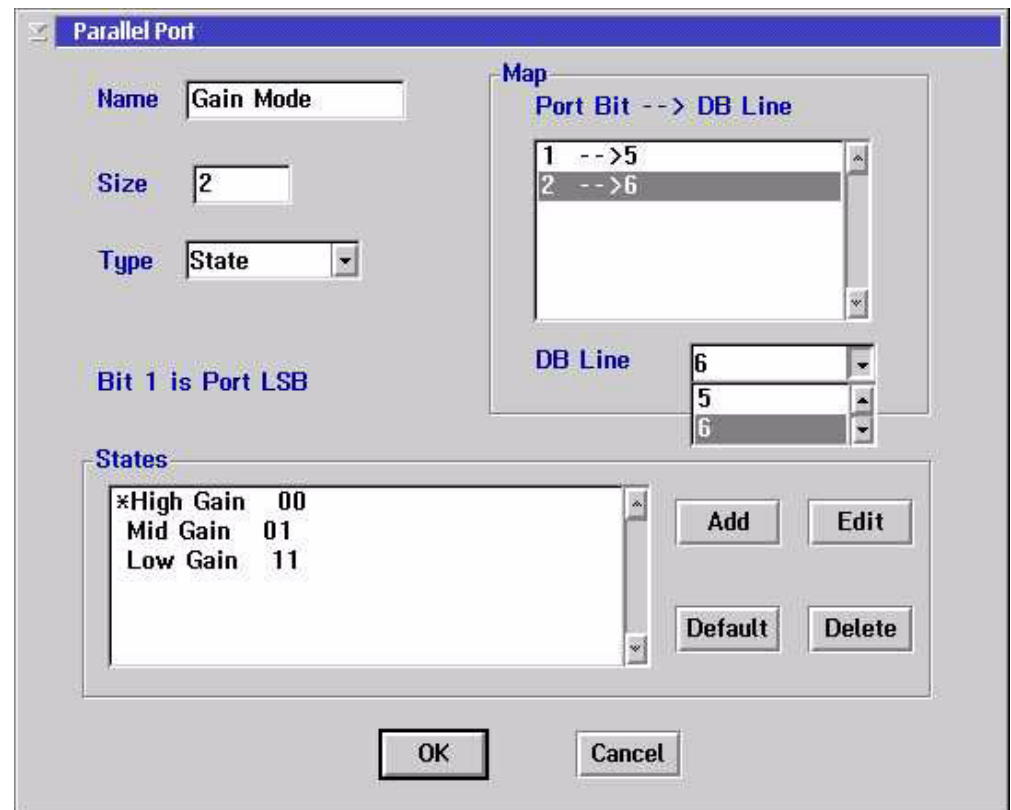
Serial/Parallel Bus Control

- DUT Defined or "Brute Force"
- DUT Defined Contained in Dut Instrument
- Single Button Programming
- Allows Descriptive Names
- DUT buttons created



Parallel Bus

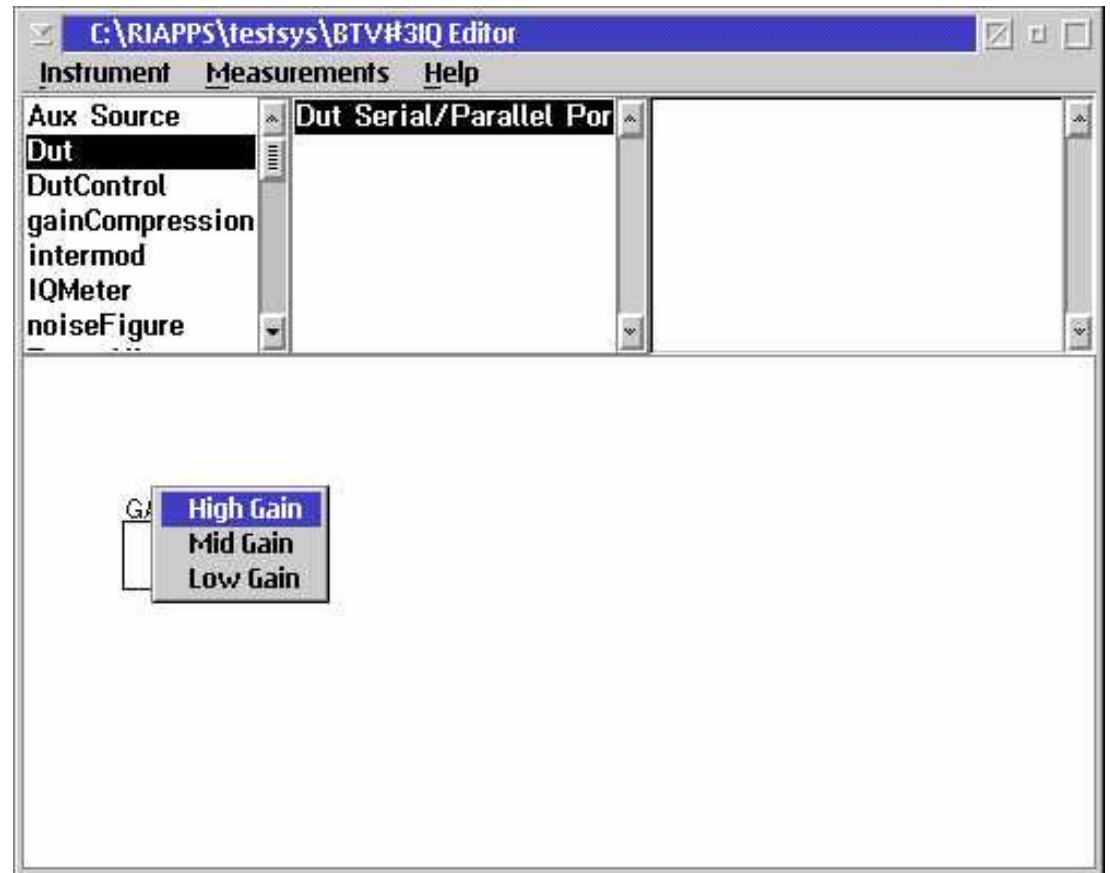
- Establish Port Size
- Set Type to State
- Map DUT pin to DB line
- Add States
- Establish Default State





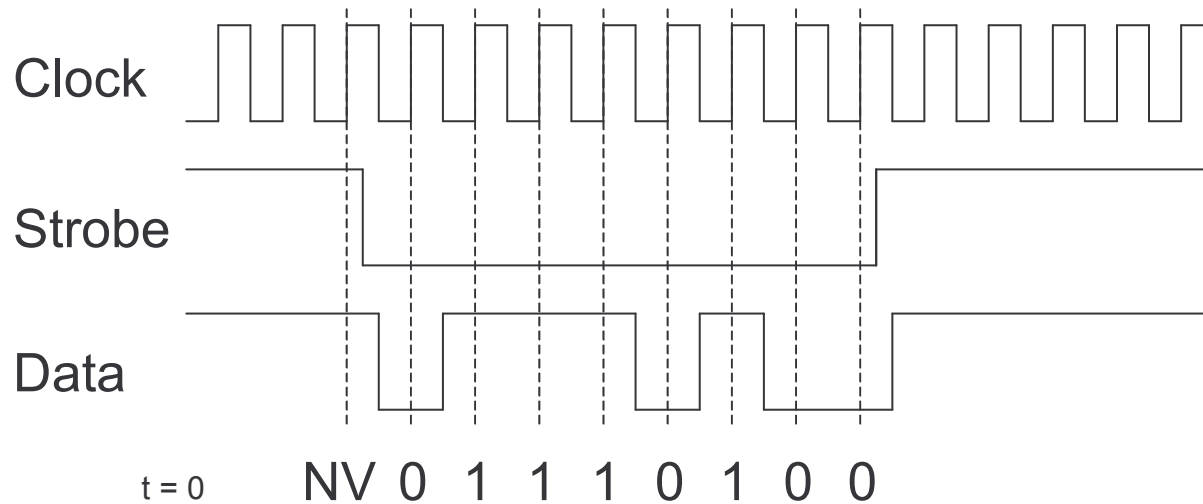
Dut Parallel Port

- Dut Object Created
- Put in Test Plan





Serial Port Basics



Data: MSB First

Clock: Positive

Strobe: Negative, Long

Data: 01110100 Binary

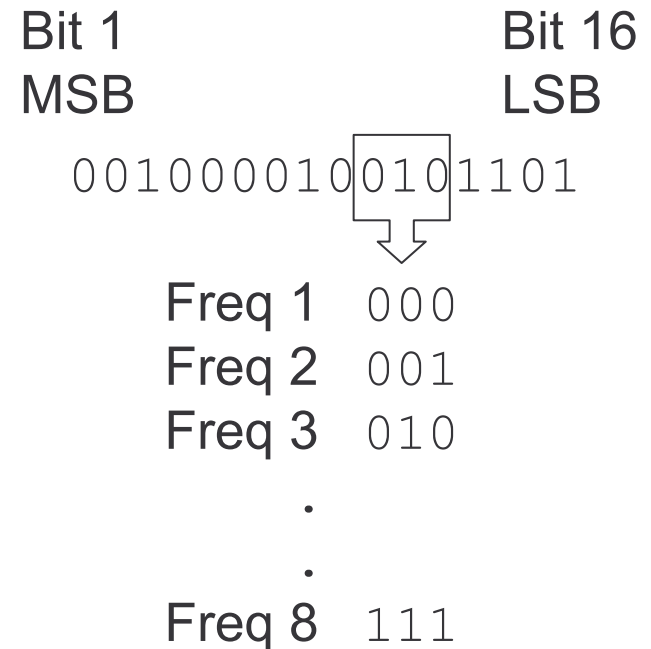
116 Integer



Serial Port Basics

Fields

- 16 Bit Bus
- Frequency Field
- 1st Bit: Bit 10
- Size: 3 Bits
- 8 Potential States





RI Serial Definitions

- Bit order 1 thru N (no bit 0)
- Bit 1 is MSB
- Bit 1/MSB is on Left

Bit 1
MSB

Bit 16
LSB

0010000100101101



Serial Port Basics

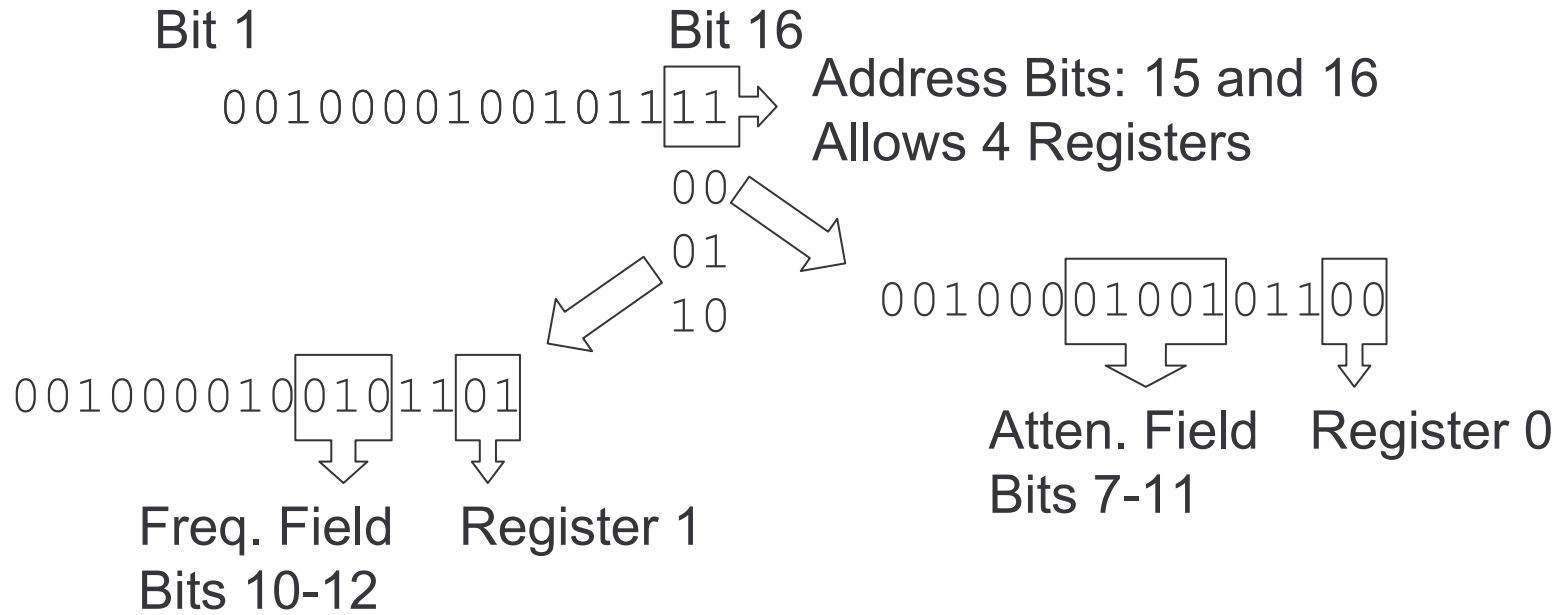
Registers

- Serial Bus can be Multiplexed into Registers
- Bits are Allocated to Register "Address"
- Specific Address Changes Field Definition
- Allows Expansion of Serial Capability



Serial Port Basics

Registers





Programming Serial Port

- Select Serial Type
 - Dut Defined/Local/I2C/I3C
- Assign Static Digital Resources
 - Clock
 - Data
 - Strobe
- Define Dut



Fast Serial Control

- Standard Serial: 60 KB/Second
- Fast Serial: Up to 2.5 MB/Second
- Fast I2C: Up to 600 KB/Second
- Specific Digital Resources
 - Read: DB 1 or 9, Write: DB 2 or 10
 - Clock; DB 3 or 11
 - Must be adjacent
- New "Serial Clock Period" Button



Static Digital Resources

- Type
- Read
- Clock
- Data
- Strobe

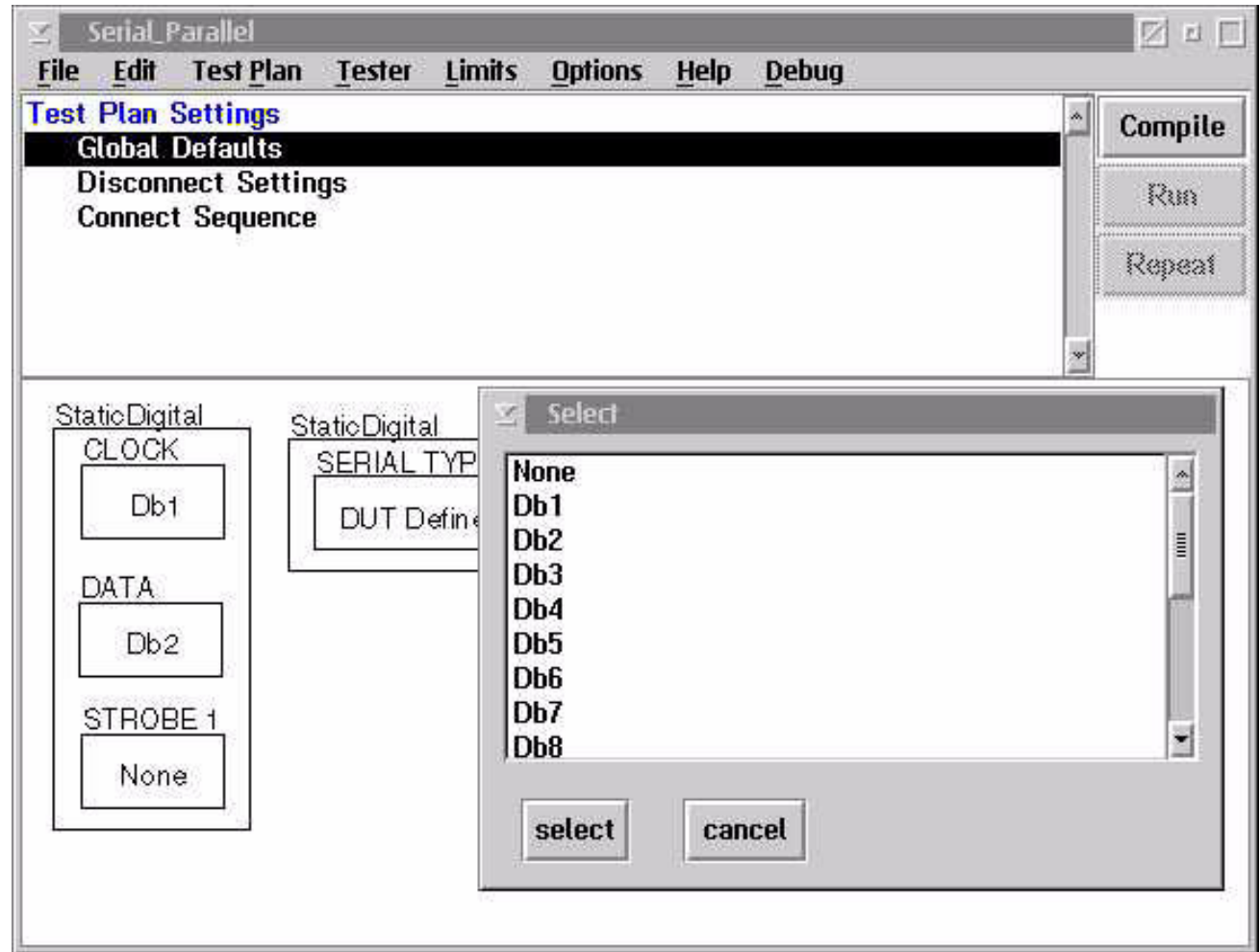
The screenshot shows the 'BTVM#3IQ Editor' window with the 'StaticDigital' resource selected. The configuration parameters are as follows:

Parameter	Value
Serial Type	DUT Defined
Clock	None
Serial Size	0
Serial Direction	msb first
Data	None
Serial Data	
Strobe 1	None
Serial Clock Polarity	positive
Strobe 2	None
Serial Strobe Polarity	positive
Serial Strobe Length	short



Static Digital Resources

- Assign DB Lines





Dut Definition

- Style
- Bit Order
- Clock
- Strobe Pulse
- Strobe Length

Serial Port

Style: serialStdFormat:

Bit Order

MSB First

LSB First

Clock Pulse

Positive

Negative

Strobe Pulse

Positive

Negative

Long

Short

Fields

Name	Register	Type
------	----------	------

Add

Edit

Delete

OK

Cancel



Register Addressing

- Register: Reg00
- Type: Constant
- Bits 15 and 16

Serial Field

Name: Reg00Addr Register: Reg00

1st Bit Location: 15 Size: 2

Type: Constant

States

00

Add Edit

Default Delete

OK Cancel



Fields in a Register

- Reg00 Links to Register 0
- Field: Starts Bit 7, 5 bits Wide
- Type: State
- Add States w/Bits
- Set Default

Serial Field

Name: Atten Register: Reg00

1st Bit Location: 7 Size: 5

Type: State

States

Min Atten	00000
x Max Atten	11111

Add Edit

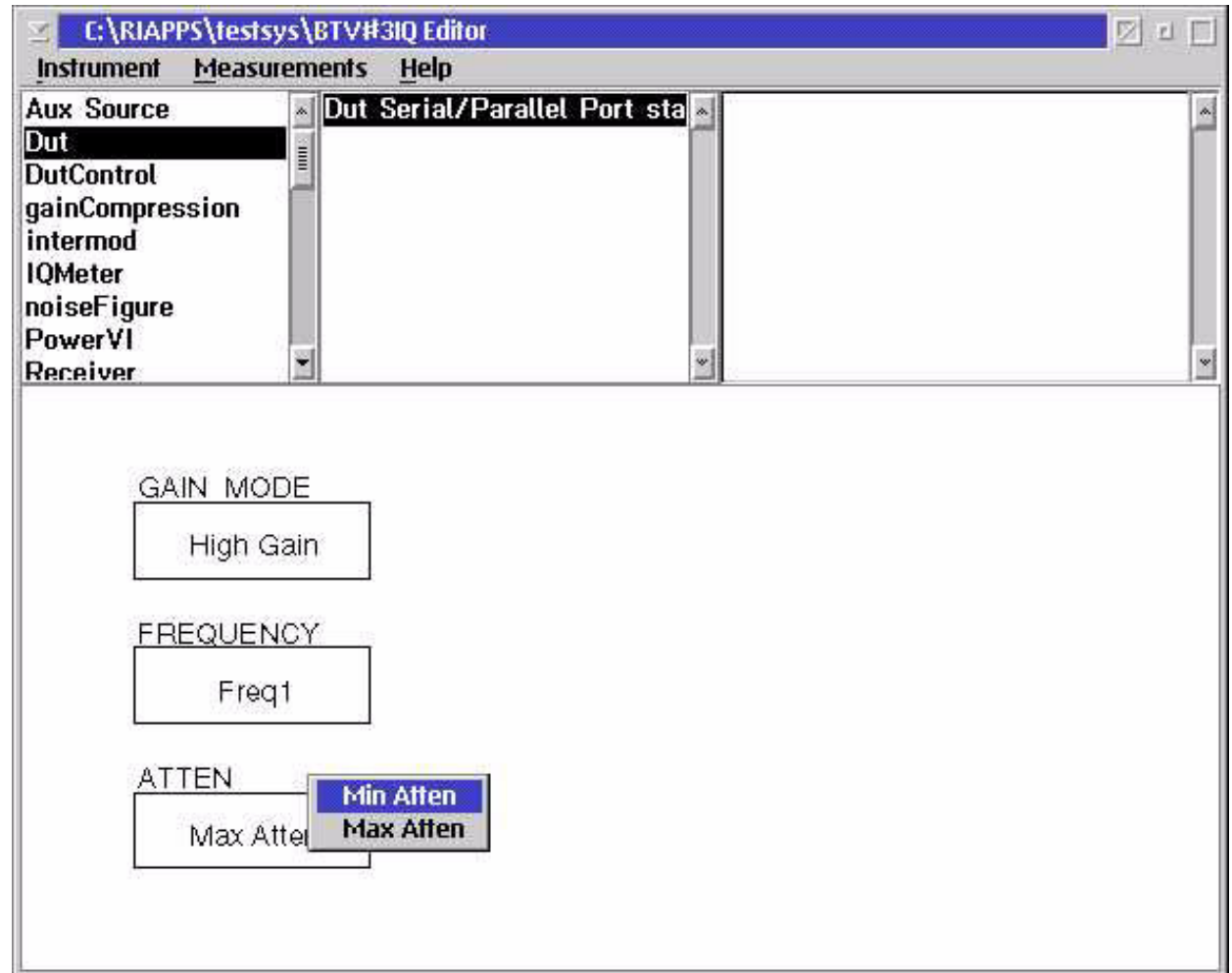
Default Delete

OK Cancel



DUT Serial Port

- DUT Created
- Put in Test Plan



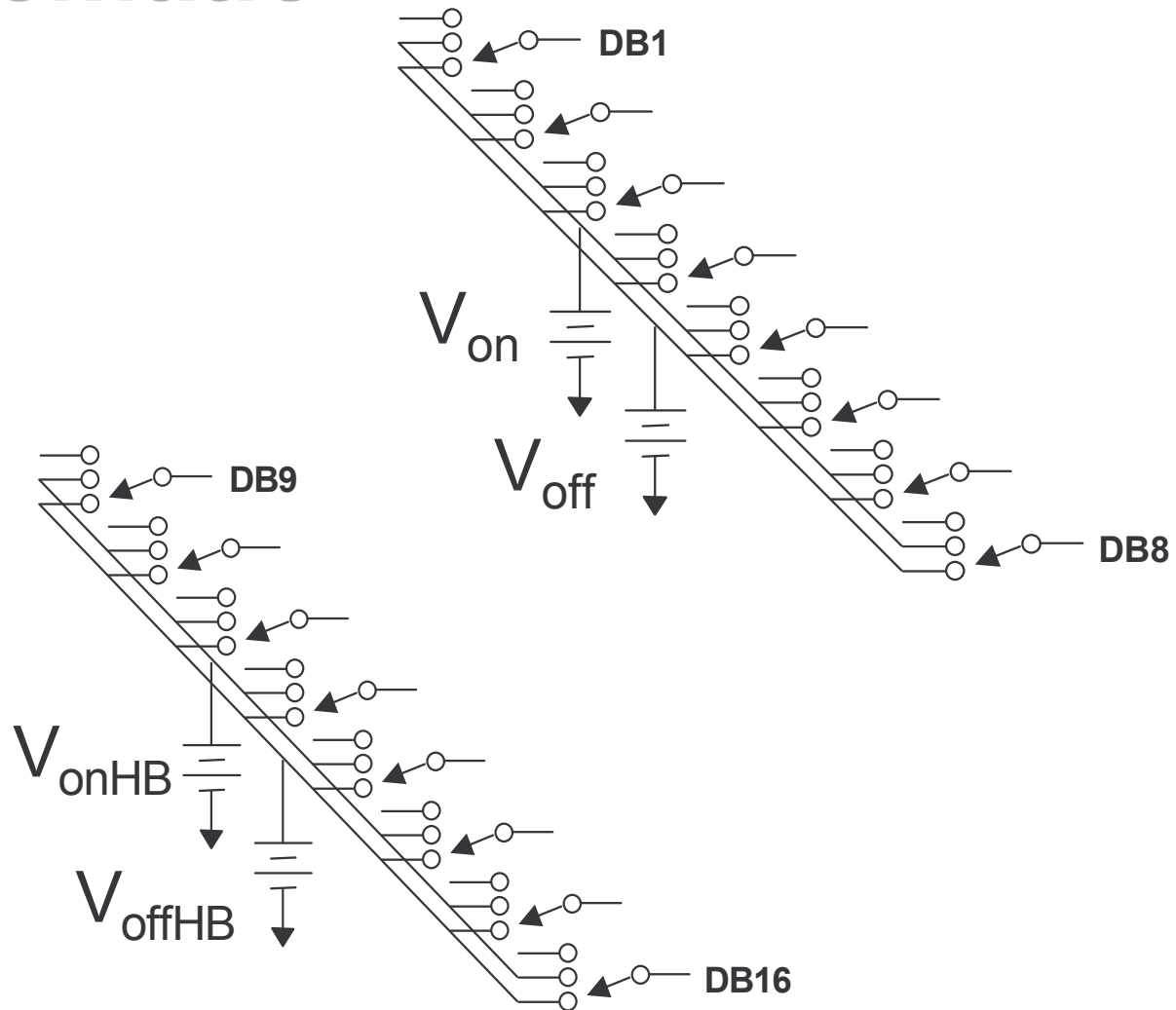


DB Lines Description

- Switch between Von. Voff, Open
- 16 lines, 2 banks
- 4 voltage supplies
- 1 Precision Multimeter
- 2 mA limit
- +/- 10V



Schematic





Measuring Leakage Current or ESD Diode Voltage with DB Lines

- Select voltage or current measure mode
- Set Opposing Limit (V or I Hard Limit)
- Set Measure Max. (sets Resolution)
- Set DB pin to Open
- Select DB pin to be Measured



Leakage Current Measurement

The screenshot shows a software window titled "DB Current and Voltage Meas" with a menu bar containing "File", "Edit", "Test Plan", "Tester", "Limits", "Options", "Help", and "Debug". The main area is divided into two sections. The top section contains a tree view of test sections: "Connect Sequence", "Test Section: DC Tests", "Conditional Statement", "Section Defaults", "Test: Low level Current Test" (highlighted in black), and "Test: ESD Diode Check". On the right side of this section are three buttons: "Compile", "Run", and "Repeat".

The bottom section displays a configuration diagram with several parameter boxes:

- StaticDigital MEASURE MODE**: Value "lmeas"
- StaticDigital MEASURE V FORCE**: Value "3"
- StaticDigital CURRENT MEAS MAX**: Value "1000 u"
- StaticDigital MEASURE I LIMIT**: Value "1000 u"
- StaticDigital MEASURE PIN**: Value "DB1"
- StaticDigital DB 1**: Value "open"
- StaticDigital MEAS**: Value "Current A"
- System SAVE AMPS**: Value "Leakage current"

A line connects the "A" unit in the "MEAS" box to the "Leakage current" value in the "SAVE AMPS" box.



Diode Voltage Check

DB Current and Voltage Meas

File Edit Test Plan Tester Limits Options Help Debug

Connect Sequence
Test Section: DC Tests
Conditional Statement
Section Defaults
Test: Low level Current Test
Test: ESD Diode Check

Compile
Run
Repeat

StaticDigital MEASURE MODE
vMeas

StaticDigital MEASURE I FORCE
1000 u

StaticDigital MEASURE I LIMIT
1000 u

StaticDigital MEASURE V LIMIT
1

StaticDigital MEASURE PIN
DB2

StaticDigital DB 2
open

StaticDigital MEAS
Voltage A

System SAVE VOLTS
Diode Voltage



Source & Measurement Performance

- Absolute Power
- Relative Power
- S parameters (Amplitude and Phase)
- Noise Figure
- Phase Noise
- Baseband (Amplitude and Phase)
- Oscilloscope/Digitizer Measurements
- DC Voltage and Current



Production Testing Typical Performance

<u>DUT</u>	<u>Measurement</u>	<u>Performance</u>
● LNA	Noise Figure	<1.0 dB
● IPA	CDMA ACPR1 CDMA ACPR2	<-60 dBc <-70 dBc
● Mixer	Noise Floor	<-150 dBm/Hz



Production Testing Typical Performance

- | <u>DUT</u> | <u>Measurement</u> | <u>Performance</u> |
|------------|--------------------|--------------------------------|
| • PLL/VCO | Phase Noise | <-115 dBc/Hz
100 kHz offset |
| • Dividers | Frequency | <1 Hz resolution
to 20 GHz |



Production Testing Typical Performance

<u>DUT</u>	<u>Measurement</u>	<u>Performance</u>
● I/Q Mod	Phase Match	<0.1 degree
	Amplitude Match	<0.025%
	LO Rejection	<-60 dBs
	Image Rejection	<-70 dBs
● I/Q Demod	Phase Match	<0.1 degree
	Amplitude Match	<0.1 dB



Selecting the Correct System Resource

- RF Resources
RF 2, 3, 6 & 7, RF 4 & 5 and RF 8
- Base Band Resources
WF 2 & 3, WF 6 & 7 and WF 8
- DC Resources
VCC 1 - 6, DP 1 - 16, VI 1 - 3 &
VM 1- 4 & 1N - 4N
- Digital Resources
DB 1 - 8 and DB 9 - 16



Defining Device, Device Interface, Fixture & Tester Resources

- Start with the Device
- Device
- DUT Board & Device Interface
- Test Fixture
- Test Head
- Tester Resources



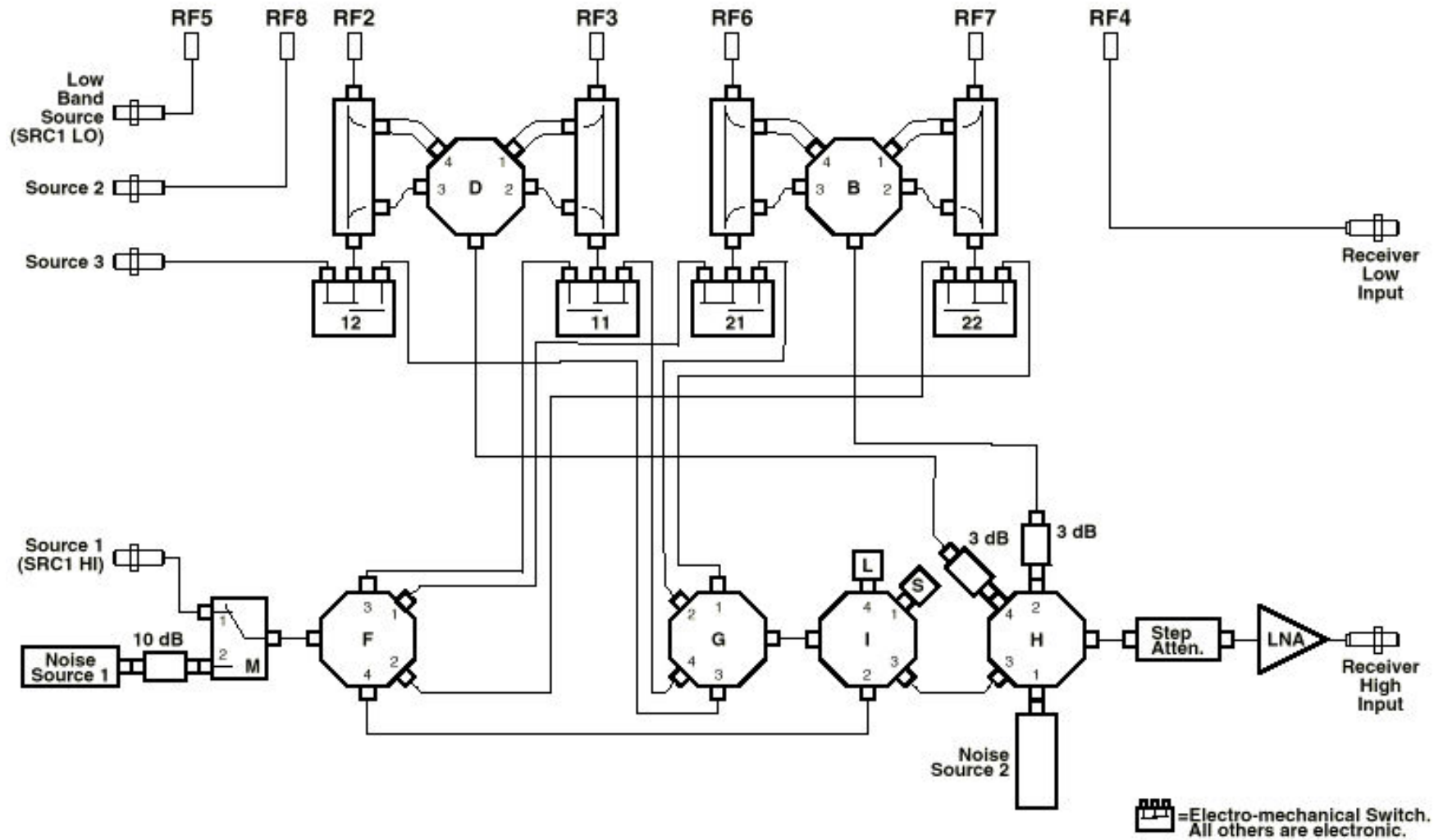
Testhead Set-Up

The screenshot shows the BTVM#3IQ Editor software interface. The title bar indicates the path: C:\RIAPPS\testsys\BTVM#3IQ Editor. The menu bar includes Instrument, Measurements, and Help. On the left, a tree view lists components: Source4, Src12Output, StaticDigital, System, Testhead (selected), vna, and Waveform. The main area is divided into two panes. The top pane shows a tree view for the selected Testhead component, with 'RF Setup' selected. The bottom pane displays a configuration grid for the testhead setup:

RF 2 src 3	SOURCE 1 RF 3	REC ATTENUATION 0db	LOAD STATE load
RF 3 receive	SOURCE 1 MODE source	RECEIVE MODE s parameters	
RF 6 receive	INPUT PORT Rf 3	PARAMETER a1	
RF 7 receive	OUTPUT PORT Rf 6		

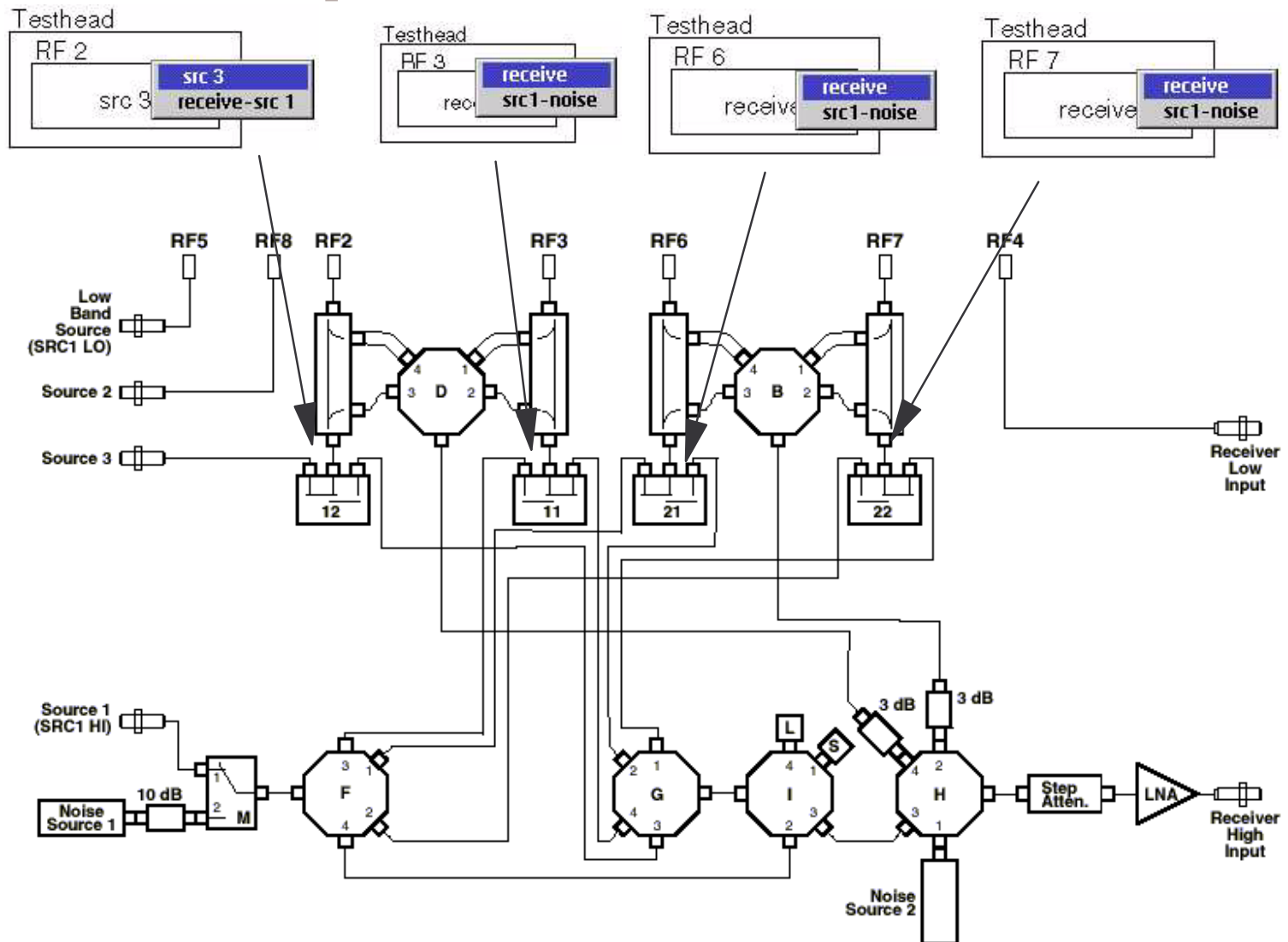
RF Block Diagram, Test Head

12/22/99



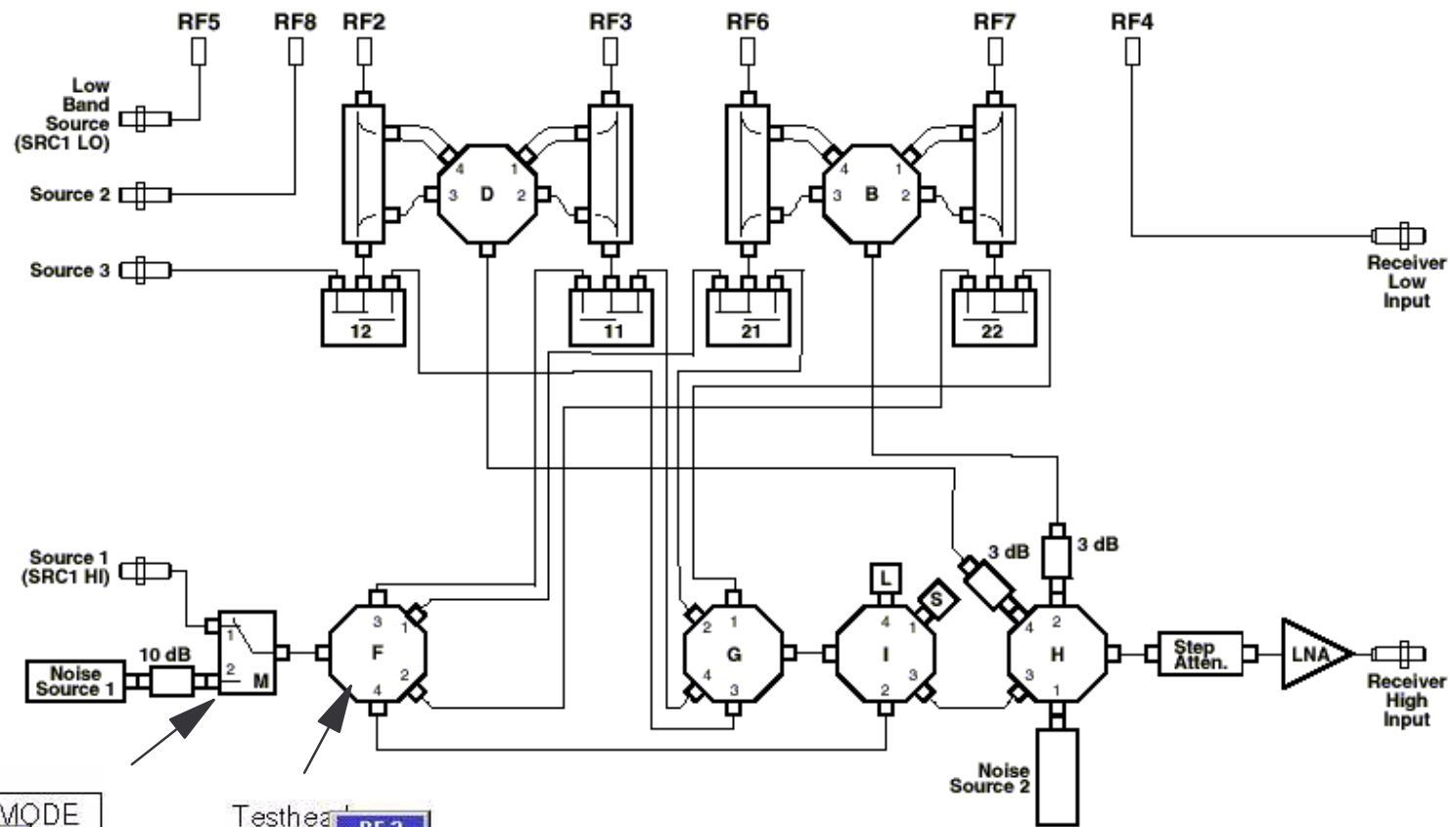


Port Set-Up





Stimulus



Testhead

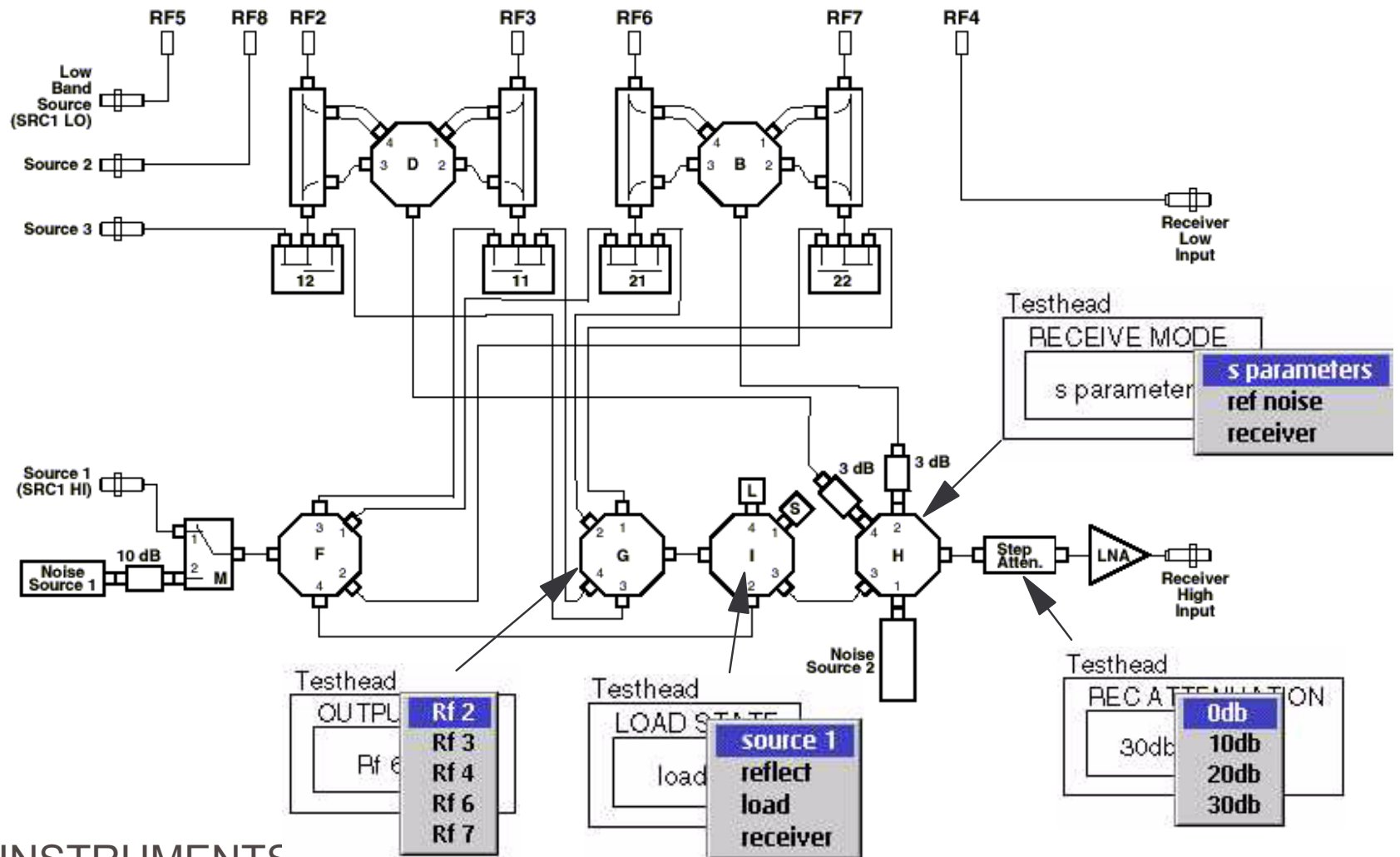
SOURCE 1 MODE
source
noise

Testhead

RF 2
RF 3
RF 5
RF 6
RF 7
Load

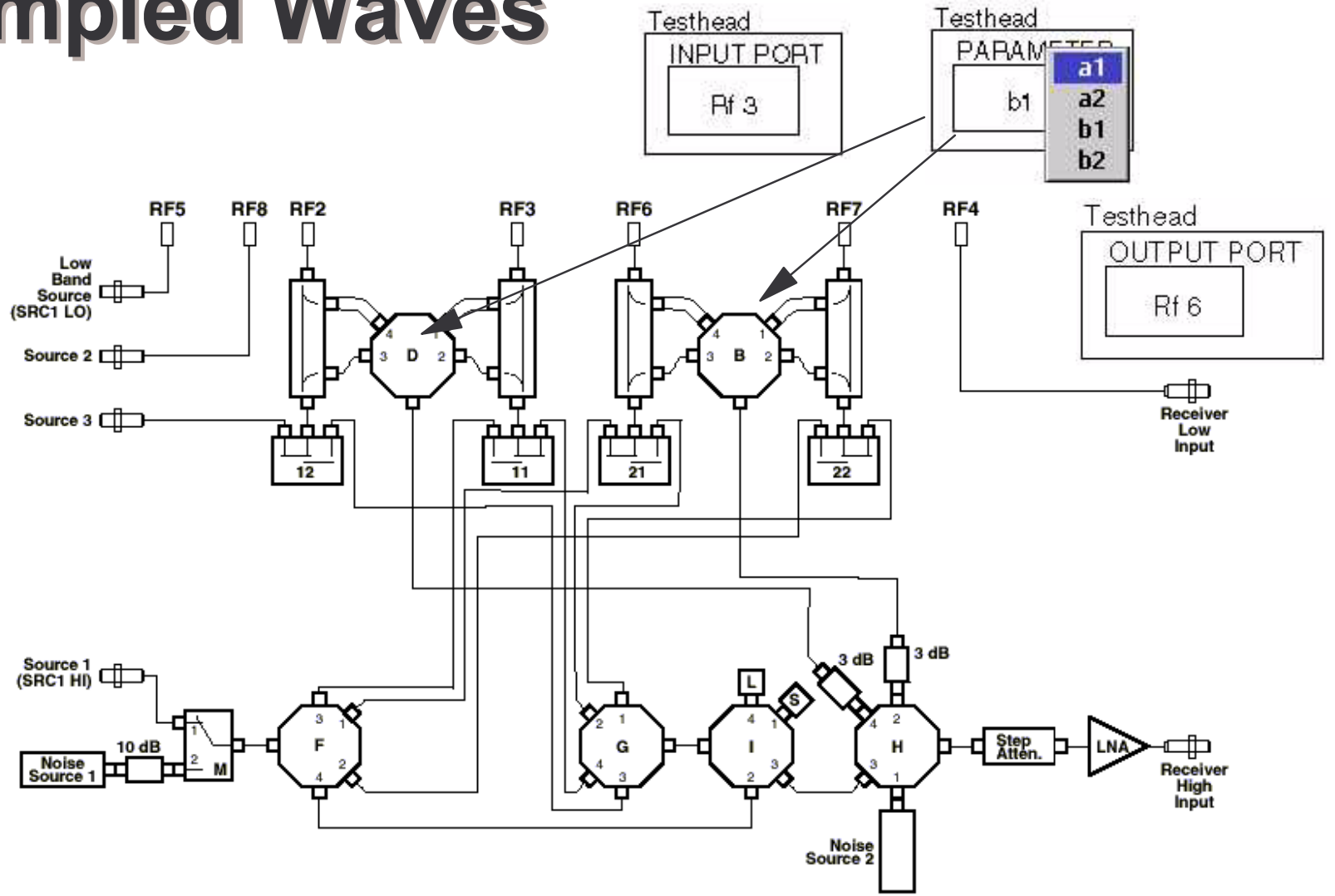


Receive





Sampled Waves





SRC12 Output

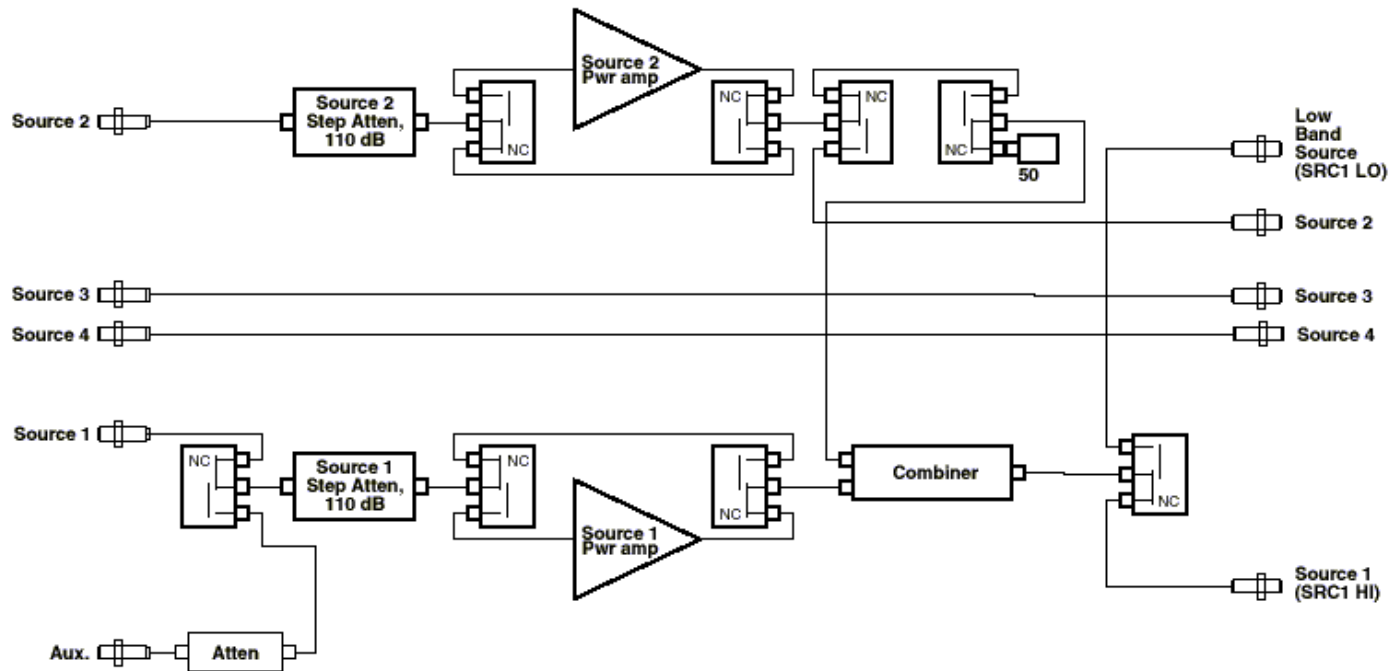
The screenshot shows the 'BTVM#3IQ Editor' software interface. The title bar indicates the file path: C:\RIAPPS\testsys\BTVM#3IQ Editor. The menu bar includes 'Instrument', 'Measurements', and 'Help'. On the left, a tree view lists various components: SineGen, Source1, Source2, Source3, Source4, Src12Output (highlighted), StaticDigital, System, Testhead, vna, and Waveform. The main area displays the configuration for 'Src12Output', with a 'state' dropdown menu at the top. The settings are as follows:

- INTERMOD TRACKING: OFF
- INTERMOD FREQ SPACING: 0 Mhz
- INTERMOD POWER SPACING: 0 db
- AUX POWER: 0 dbm
- SOURCE 1 ATTN: 0db
- SOURCE 1 AMP: OFF
- SOURCE 2 ATTN: 0db
- SOURCE 2 AMP: OFF
- SOURCE OUTPUT MODE: Combined to src 1
- SOURCE 1 OUTPUT MODE: high band



SRC12 Output

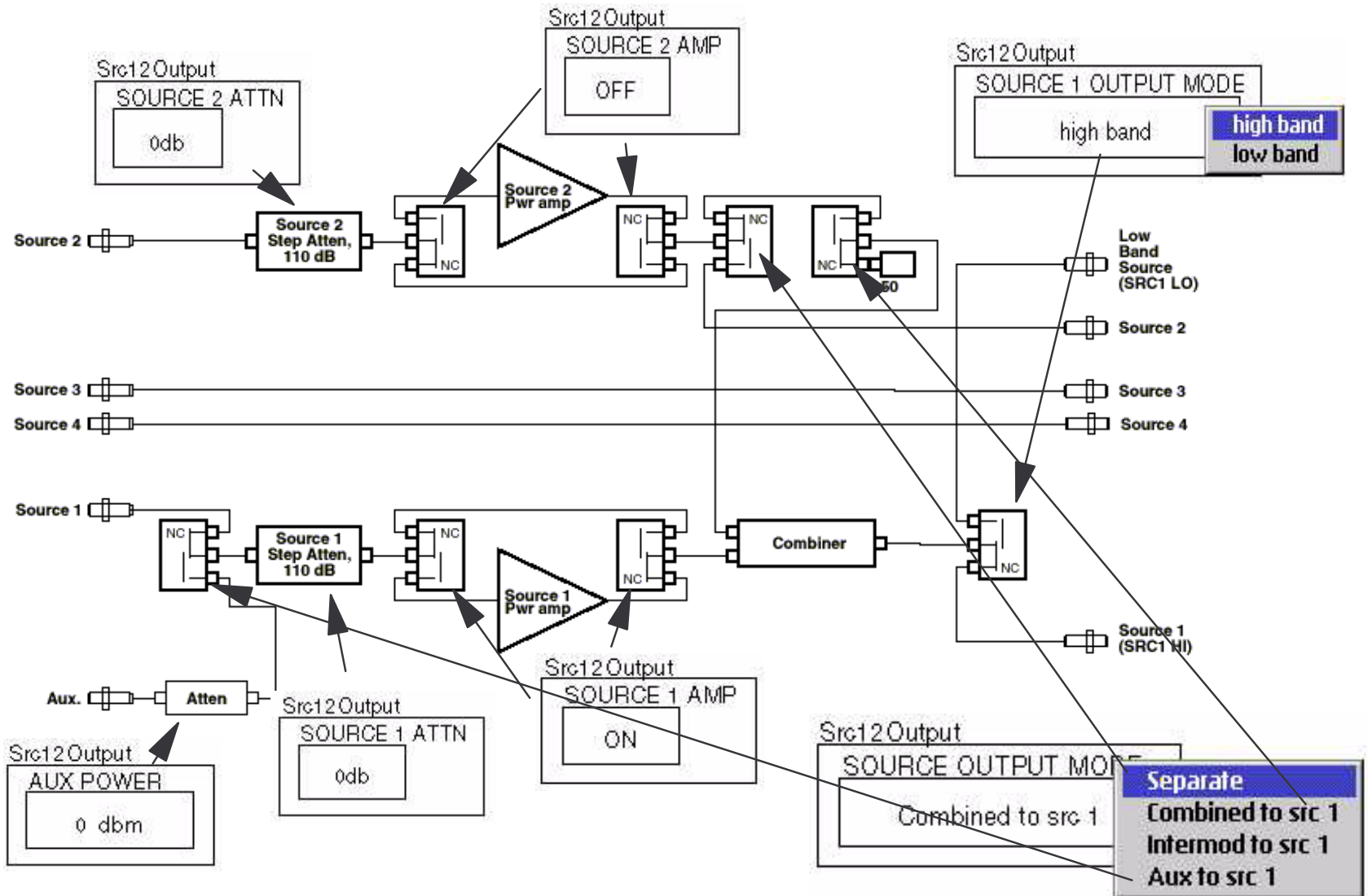
Roos Instruments, Inc
Block Diagram, Source 1/2 Output Module
RI726XA
12/22/99



Notes:
7266A: No pwr amps, no aux atten.
7267A: No aux atten.
7268A: No pwr amps
7269A: Fully loaded



SRC12 Control





Receiver State

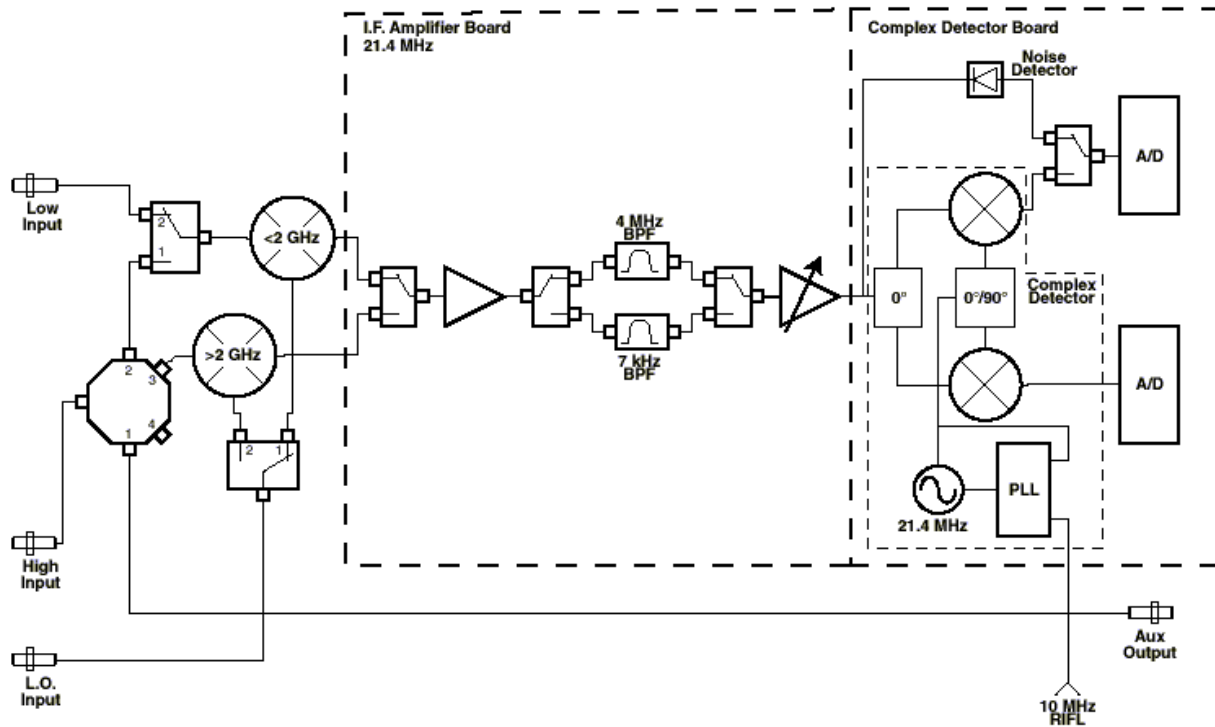
The screenshot shows the 'Receiver' state configuration in the BTVM#3IQ Editor. The window title is 'C:\RIAPPS\testsys\BTVM#3IQ Editor'. The menu bar includes 'Instrument', 'Measurements', and 'Help'. The left sidebar lists various components: noiseFigure, Oscilloscope, PowerVI, Receiver (selected), RecLo, SineGen, Source1, Source2, and Source3. The main area displays the following parameters:

Parameter	Value
FREQUENCY	1000 Mhz
MIX SIDE	high
IM SPACING	1 Mhz
INPUT	.1 - 2 (.1 - 20 input)
SAMPLES	1
IF BW	4 Mhz
MEAS RATE	20000 Hz
IF GAIN	0



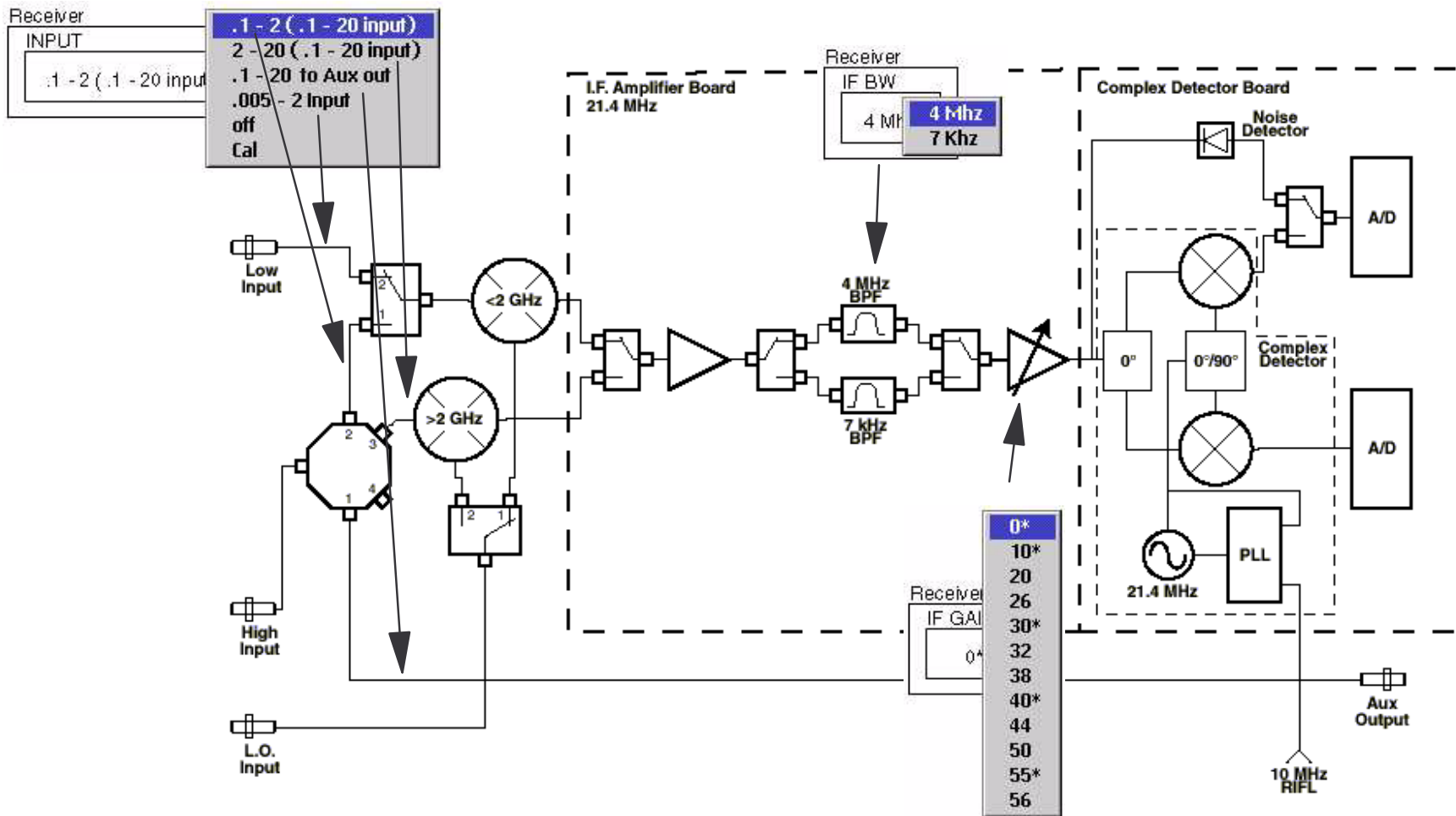
Receiver Block Diagram

Roos Instruments, Inc - RI7100A
Block Diagram, Receiver,
RI7322A
12/22/99



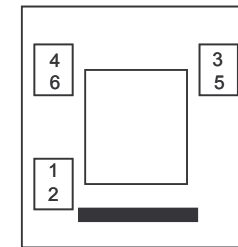
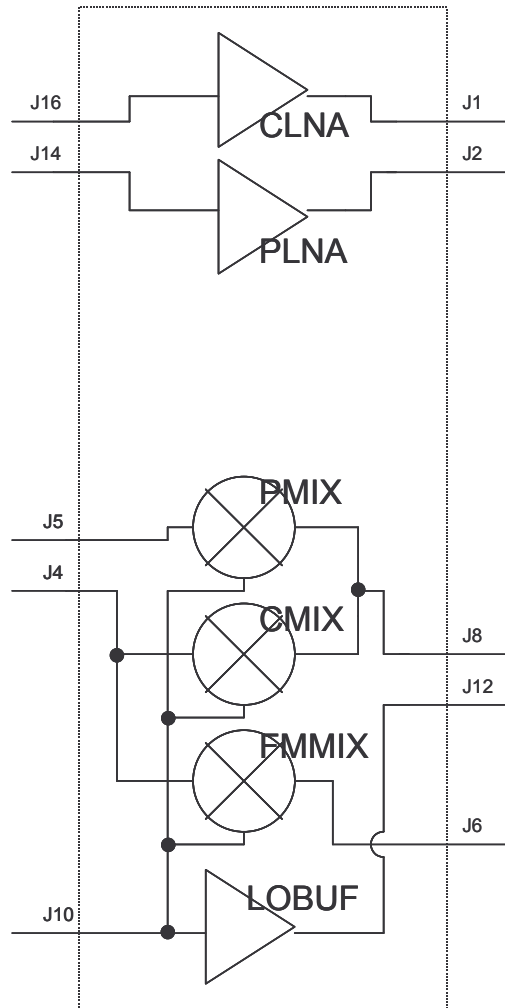


Receiver Control



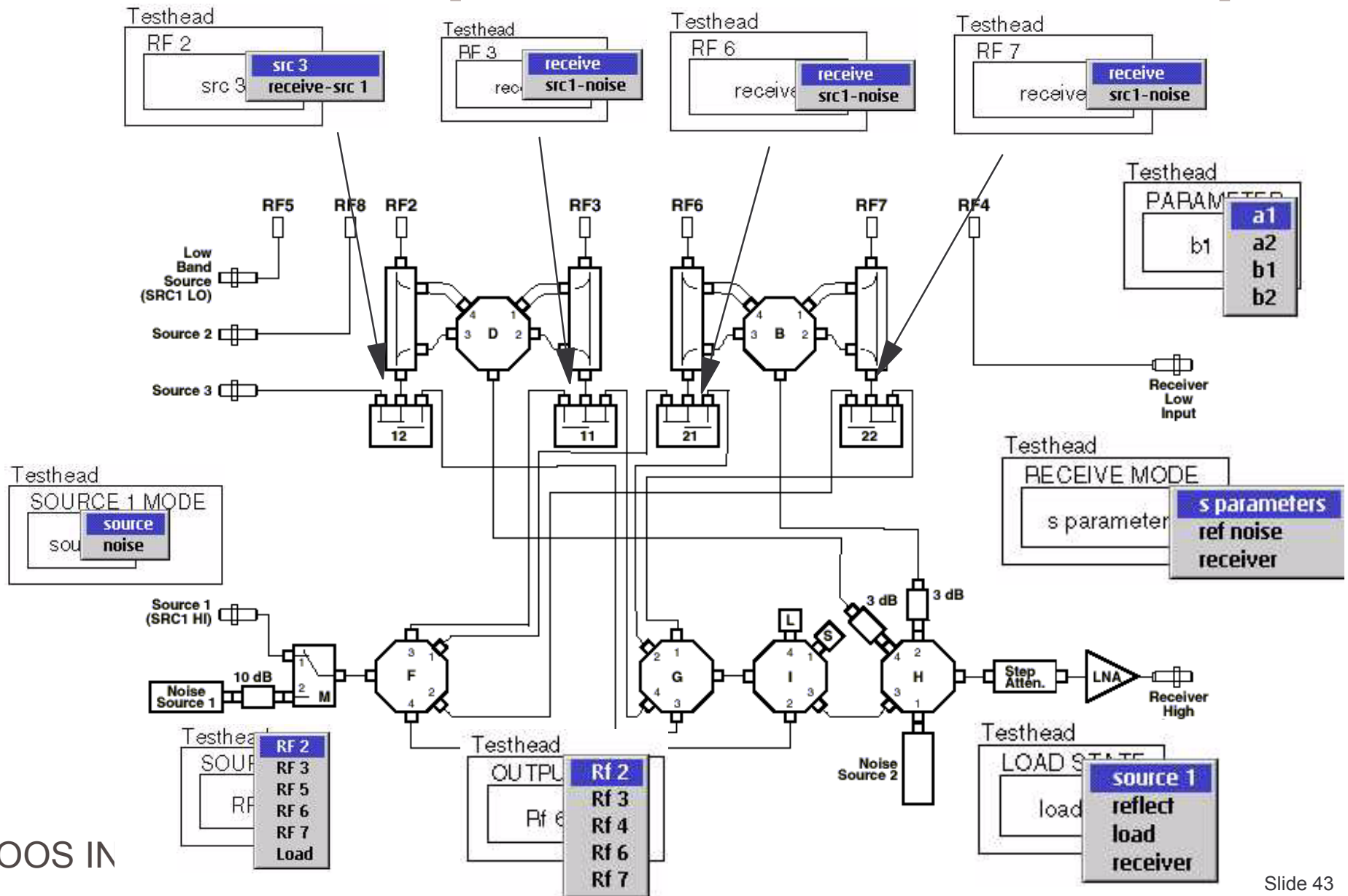


In Class Exercise - Define the Fixture & Tester Resources



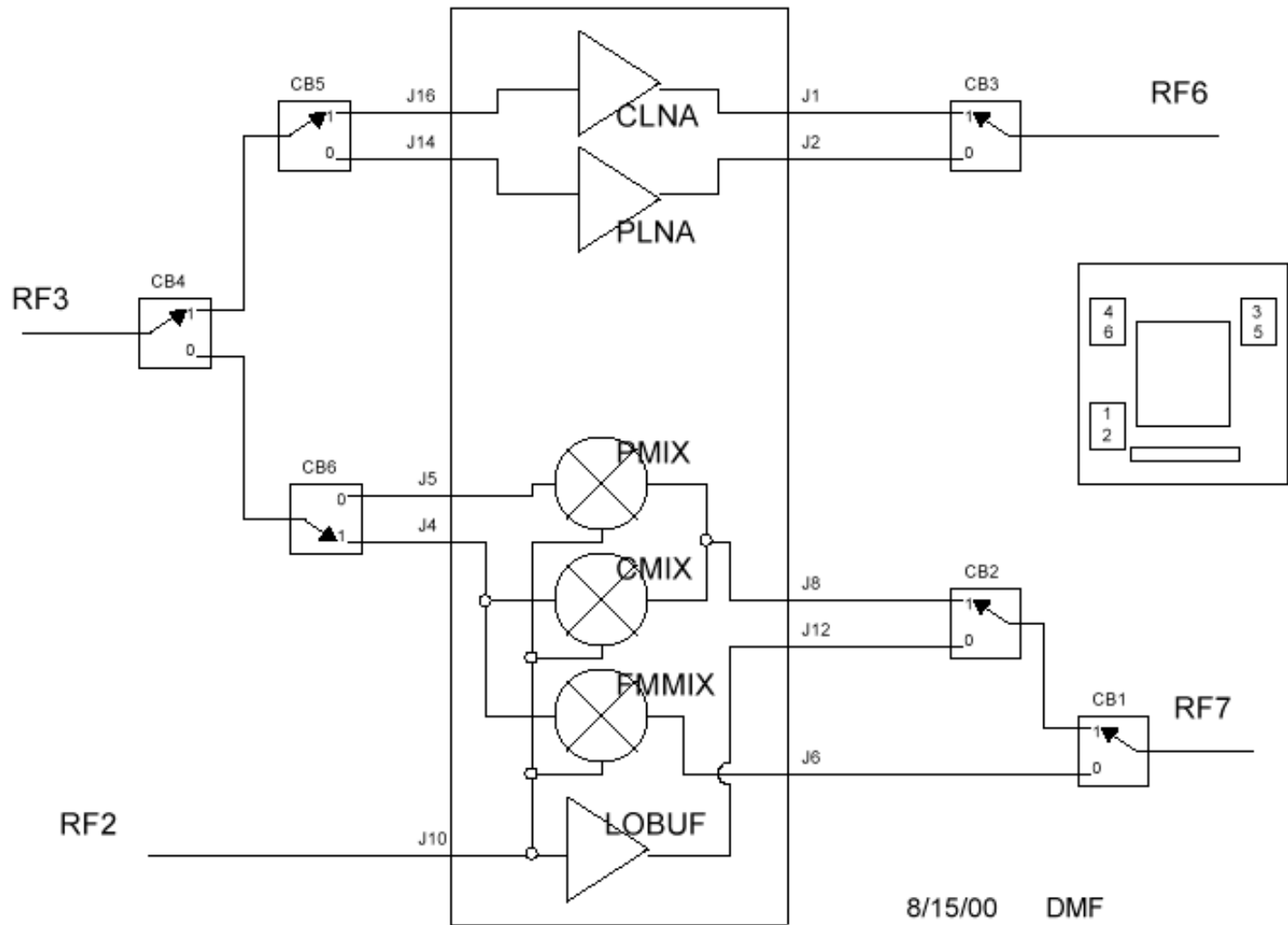


Class Example - Test Head Set-Up





Test Fixture Example



8/15/00 DMF



Test Plan - Comments, Guidelines and Suggestions

- Optimizer - Optimizes over Test Section
- Tester Viewer - Tester Reset Conditions
- Only add state buttons that are needed
- Changes cost time and money
- Data is displayed in the order listed & not displayed in the order performed
- Parameters set by LVs must be reset in the Disconnect Settings panel



Test Plan - Comments, Guidelines and Suggestions

- The tester is very fast changing state
- Your part may not be fast, add Pauses
- The tester will find unstable DUT states



Test Plan - Comments, Guidelines and Suggestions

- Fewer Test Sections better than more
- More simple test panels are better than fewer complex test panels
- Duplicate test states/conditions when ever possible
- Be consistent about where you place buttons in a test panel



Test Plan - Comments, Guidelines and Suggestions

- IMD Tests - more Receive Attn is better
- Noise Figure - Use 0 dB Rec Attn.
- Set DB Current Limit = DB I Meas Max.
- Set VI Current Limit \geq VI I Meas Max.
- RF Sources - Optimum levels +/-5 dBm
- DMSG - Optimum levels <-5 dBm
- RF Off is <-30 dBm



Organizing Your Test Plan

- Define 1st RF state in Global Defaults
- Add Fixture ON to Global Defaults
- Define general test conditions in Section Default Panels
- Define DC tests in 1st or last Section which require the RF Sources to be off
- Define DC tests in 1st or last Section which require the DUT to be turned off



Organizing Your Test Plan

- Define special startup sequences in the Connect Sequence panel or in the 1st Test Section
- Write the tests in the order listed on your test list



In Class Exercise

- List different ways to Speed-up your Test Plan



Speeding-up Your Test Plan

VCC Changes & DC Measurements: < 2 msec.

RF Measurements: <30 msec.

RF Frequency Moves: <20 msec.

Switching RF Mechanical Switches: >30 msec. & Expensive

Minimize RF Source and Receiver Frequency Moves

Minimize/Eliminate RF Mechanical Switch Changes:

- Changing RF Ports from Source to Receive or Receive to Source

- Changing RF Source 1 and RF Source 2 RF Attenuators

Wide IF Filter Measurements are faster than Narrow IF Measurements

Typically use 16 or less Averages for RF Measurements

Typically use 32 or less Averages for DC Measurements

Fast RF Measurements: S parameters, RF Power and Phase

Slow RF Measurements: ACPR, Noise Figure, Intermods & Harmonics

Setting a Parameter to a Local Variable Value Requires a Mini-Compile



Speeding-up Your Test Plan

The Optimizer only Optimizes the Tests in a Test Section

Oscope vs. Receiver Measurements

If the RF Receiver can make the Measurement, use the Receiver
Receiver is faster with better Frequency Range & Dynamic Range

Oscope is designed to measure Pulse Characteristics:

Rise/Fall Time, Period, Duty Cycle, etc.

Receiver is designed to measure Complex Signals:

Amplitude, Phase, Noise, Power, Frequency, etc.

Items to Set in Global Defaults

Receiver Frequency Tracking to Source 1 or System

Test Head Parameter to b2

RF Ports to Receive or Source

Receiver IF Gain

Source 1 Frequency & Level to first RF Stimulus Signal

Source 2 Frequency & Level to the first IM Stimulus Signal

Source 3 Frequency & Level to the first LO Stimulus Signal



Speeding-up Your Test Plan

Turning On and Off a RF Source is fast

Switching Source 1 Mode to Noise is faster!

Use Source 1 Mode button to Isolate Source 1 & 2 from DUT

Don't use Source 1 & 2 Attenuation to Isolate Source 1 & 2 from DUT

Use b1 to measure LO Leakage at the DUT's RF Input

Use Source 1 "back door" for S22 Measurements

Look at Compiled Delta Settings to Improve Test Speed

Look for changes in Receiver & Source Frequency, Attenuator & Test Head Settings, etc.

Minimize Test State changes by making test conditions exactly the same for as many measurements as possible including: RF Stimulus Levels, Frequencies, Receiver Settings, DC Levels, Current Limits, Ranges, Etc.

For IM measurements, leave RF Source 1 at the standard stimulus Frequency, this saves 2 RF Frequency Moves

Remember DC measurements set the Receiver and the RF Sources to their Default Frequencies